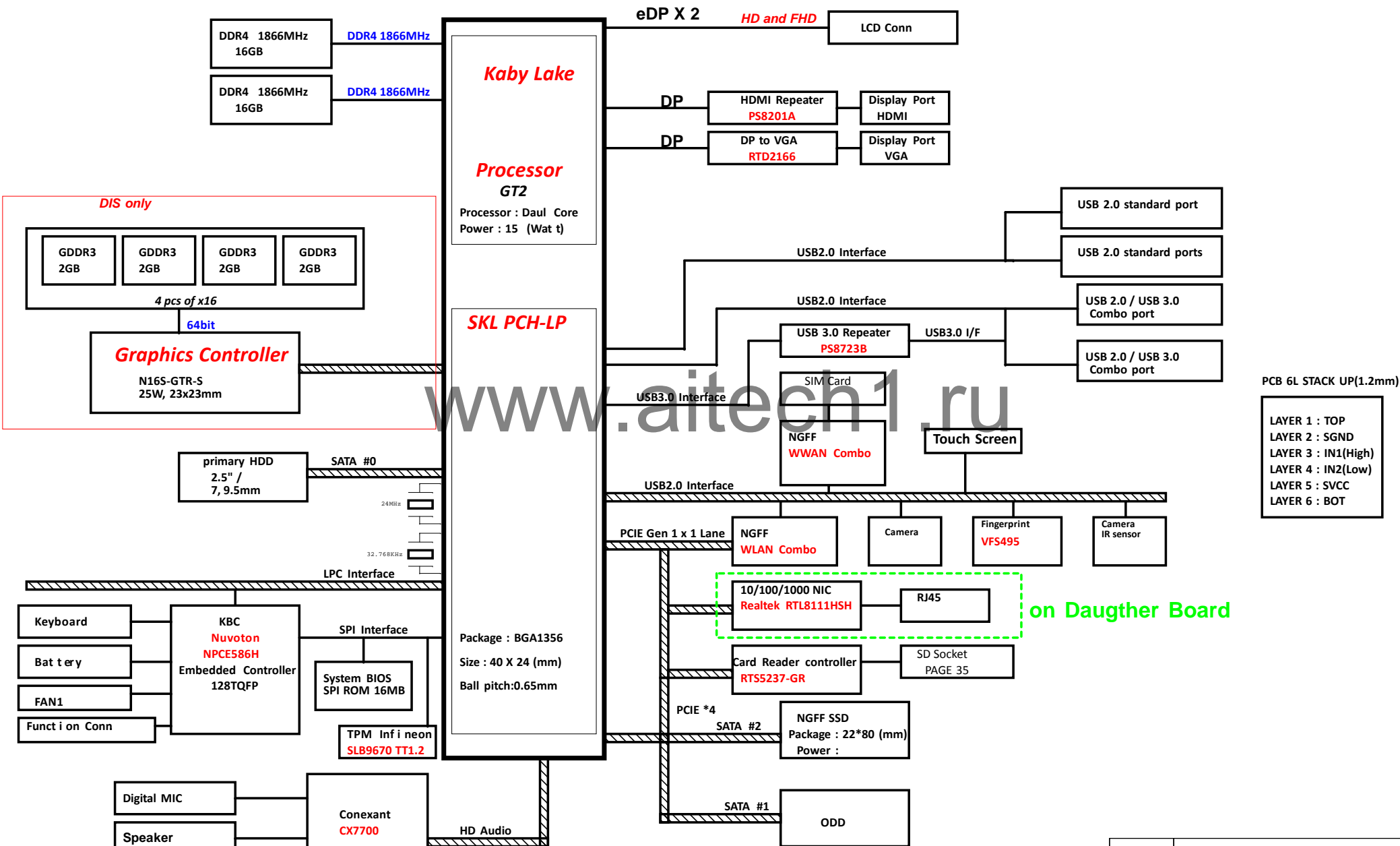
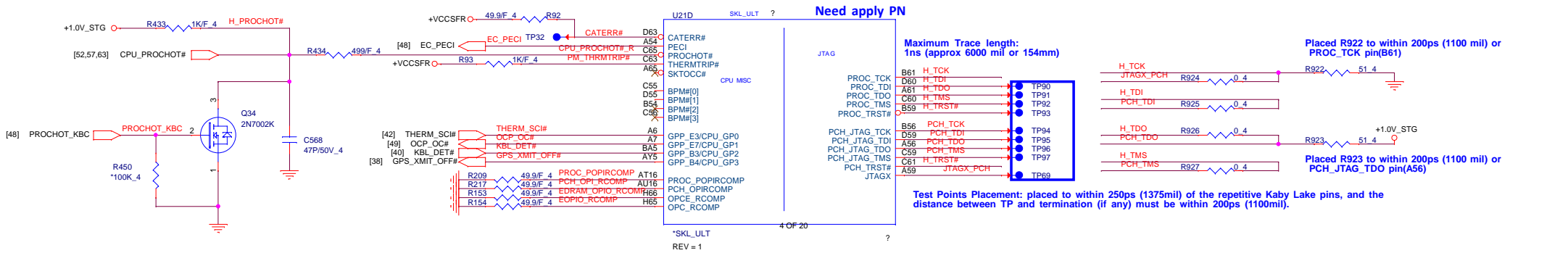
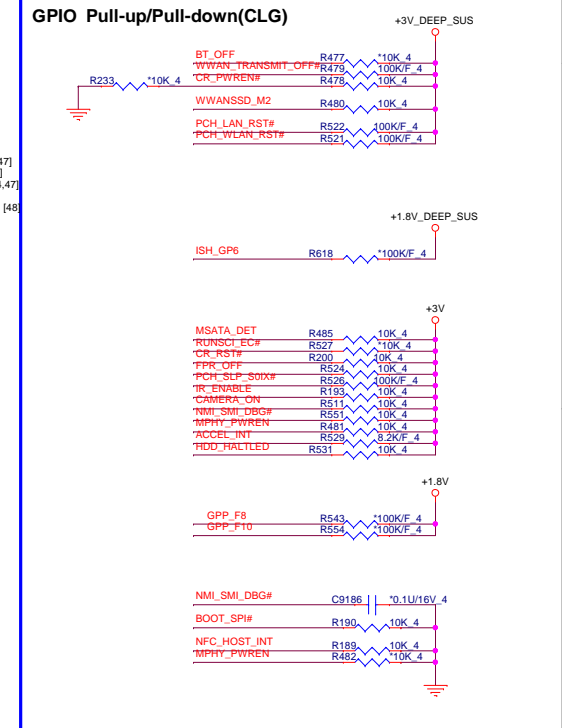
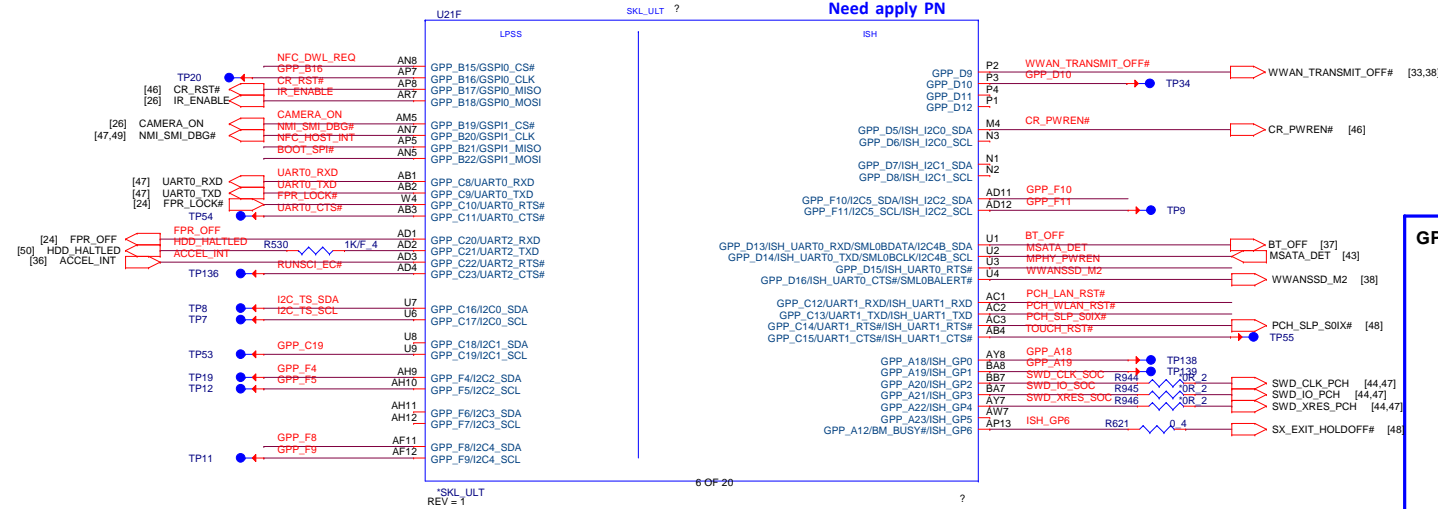


2015 400 series Kaby Lake 15"/ 17" (UMA/DIS) Block Diagram 01





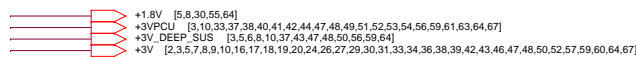
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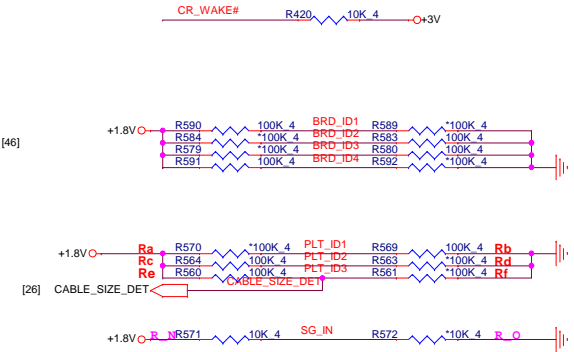
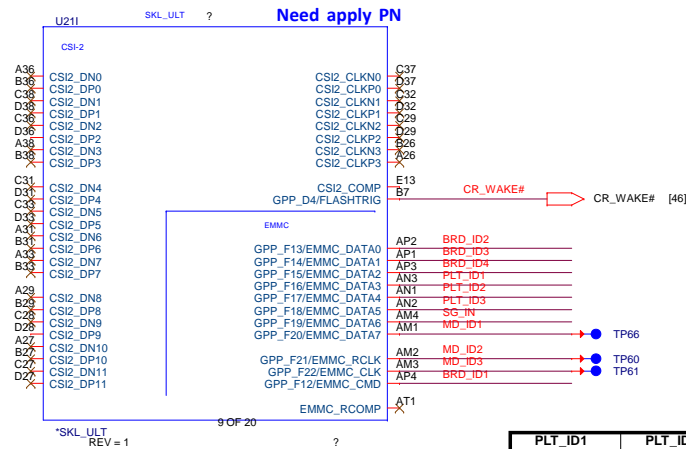
www.aitech.ru

Conexant CX7501 & CX7700 TABLE (SI stage)

	CX7501	CX7700
Rc	UNINSTALL	INSTALL
Rd	INSTALL	UNINSTALL



	BRD_ID1	BRD_ID2	BRD_ID3	BRD_ID4	
	GPIO201	GPIO202	GPIO203	GPIO204	AMD_FCH
	GPIO14	GPIO34	GPIO35	GPIO40	PPMT
	GPIO15	GPIO34	GPIO35	GPIO40	LPI-H
BOARD REVISION	GPIO76	GPIO77	GPIO78	GPIO79	LPT-LP
DB0	0	0	0	0	
DB1	0	0	0	1	
DB2	0	0	1	0	
	0	0	1	1	
SI	0	1	0	0	
SIB	0	1	0	1	
SI2	0	1	1	0	
	0	1	1	1	
Pre-PV	1	0	0	0	
PV	1	0	0	1	
	1	0	1	0	
	1	0	1	1	
MV1	1	1	0	0	
	1	1	0	1	
	1	1	1	0	
	1	1	1	1	



PLT_ID1	PLT_ID2	PLT_ID3	
Ra	Rc	Re	H
Rb	Rd	Rf	L
0	0	0	13.3"
0	0	1	14"
0	1	1	15.6"
0	1	1	17.3"

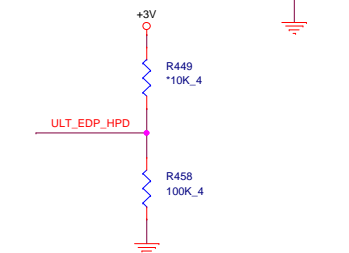
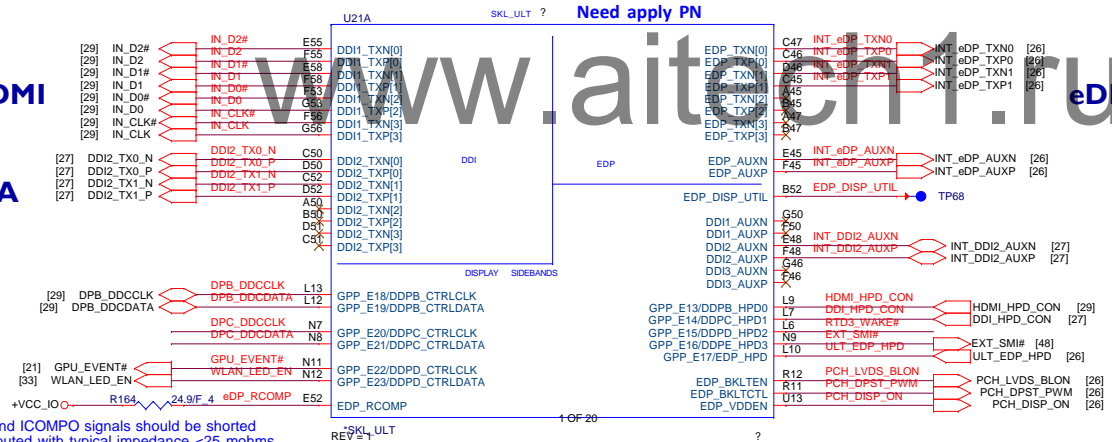
Cable detect

SG_IN	Install	Un-Install
UMA	R572 R_O	R571 R_N
DIS	R571 R_N	R572 R_O

HDMI

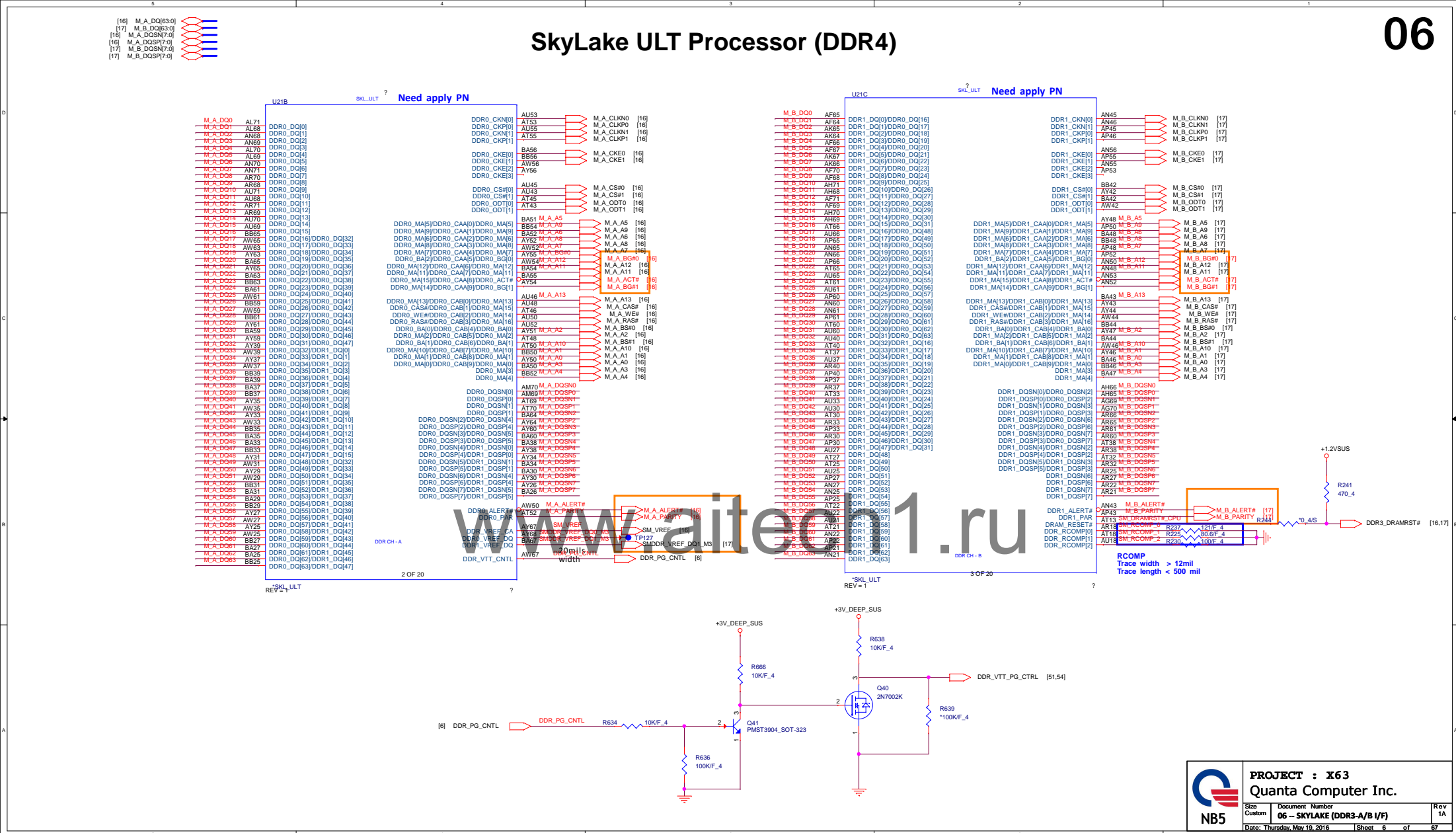
VGA

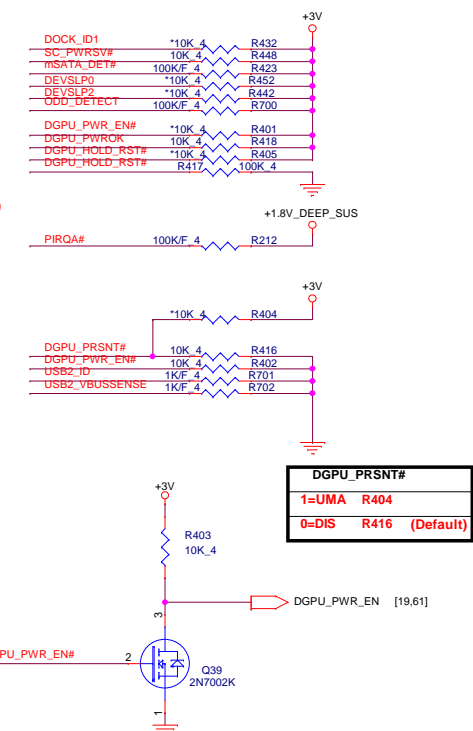
eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

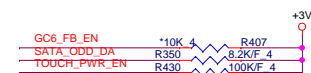
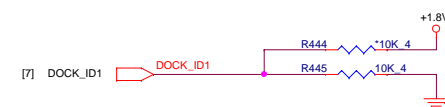
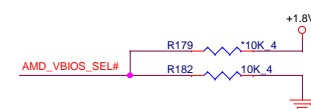
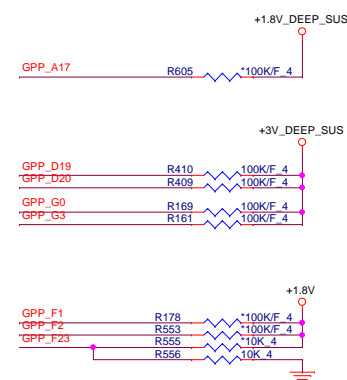
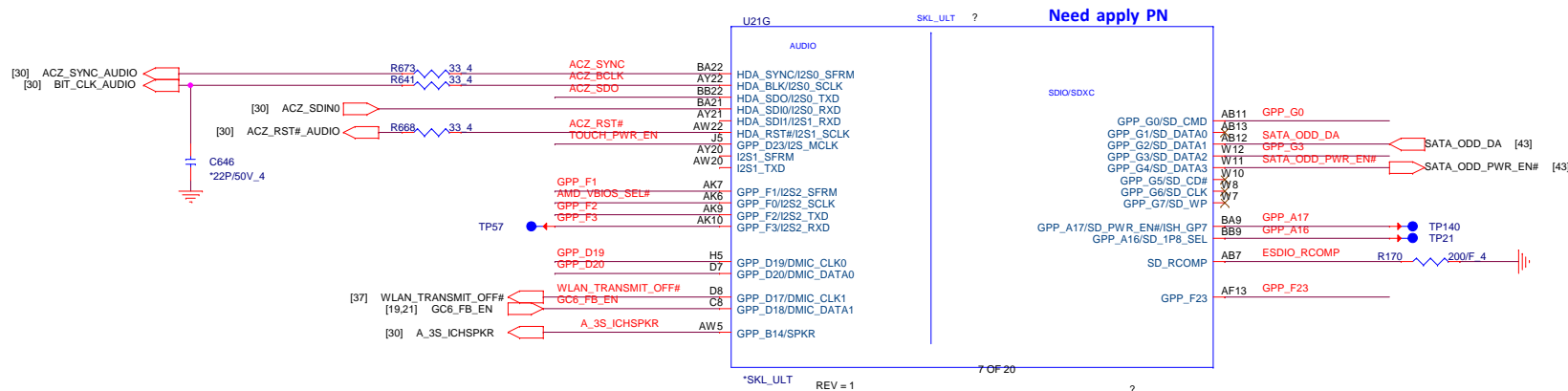


PROJECT : X63
Quanta Computer Inc.

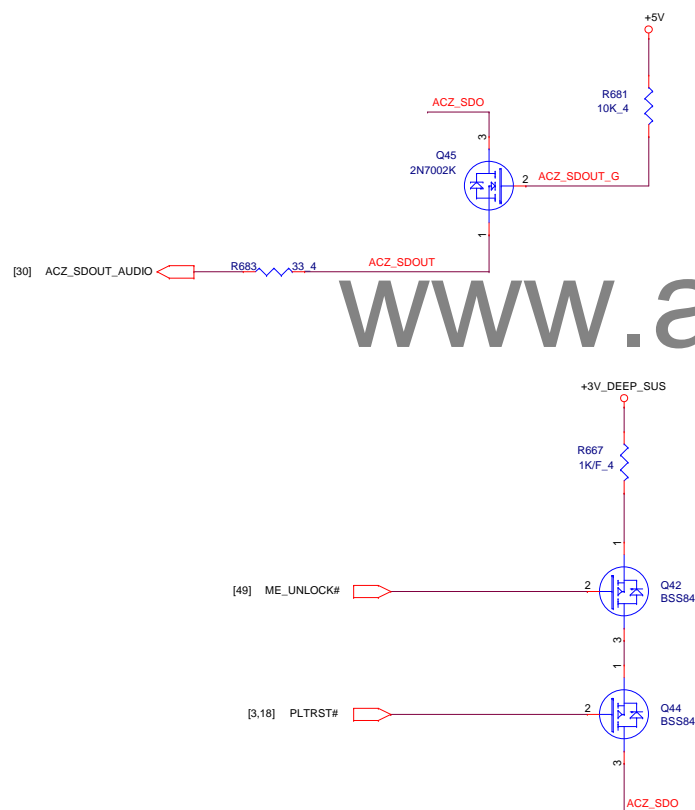
Size	Document Number	Rev
Custom	05 - SKYLAKE (eDP/DDI/Board ID)	1A
Date: Thursday, May 19, 2016	Sheet 5 of 67	





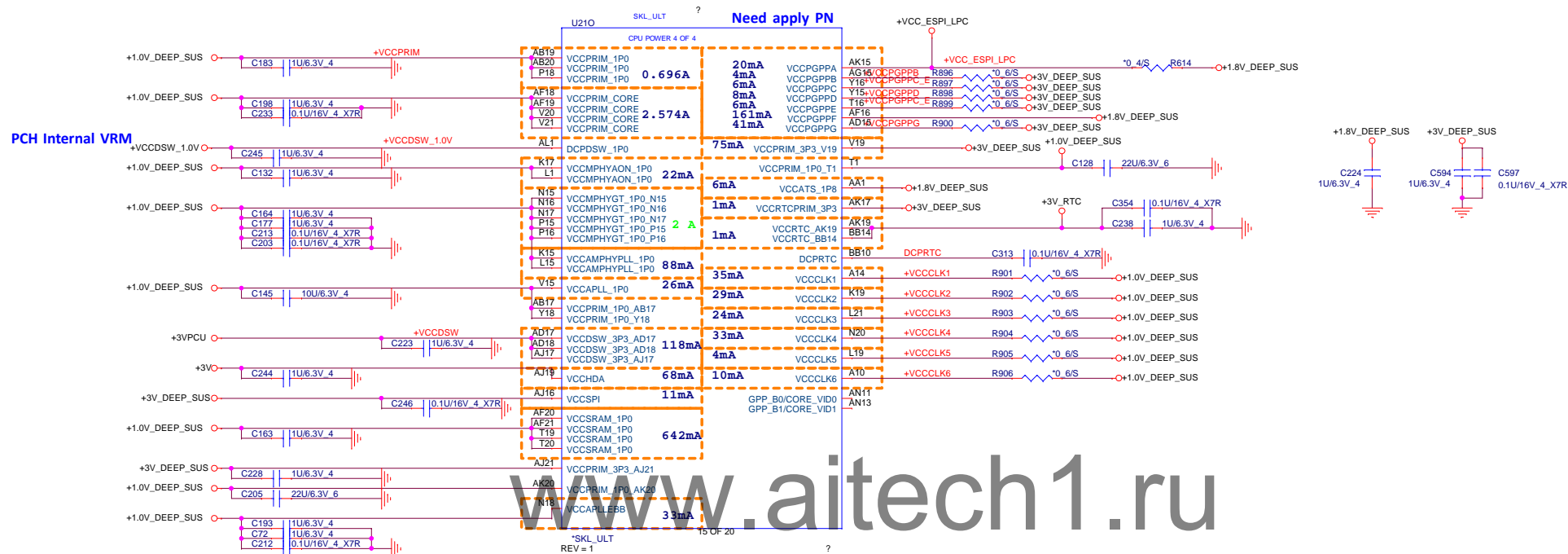


AMD_VBIOS_SEL#	DOCK_ID1
00= VBIOS 1	
01 = VBIOS 2 (Reserve for new die)	
10 = VBIOS 3 (Reserve for new die)	
11=UMA	



D

[illegible]

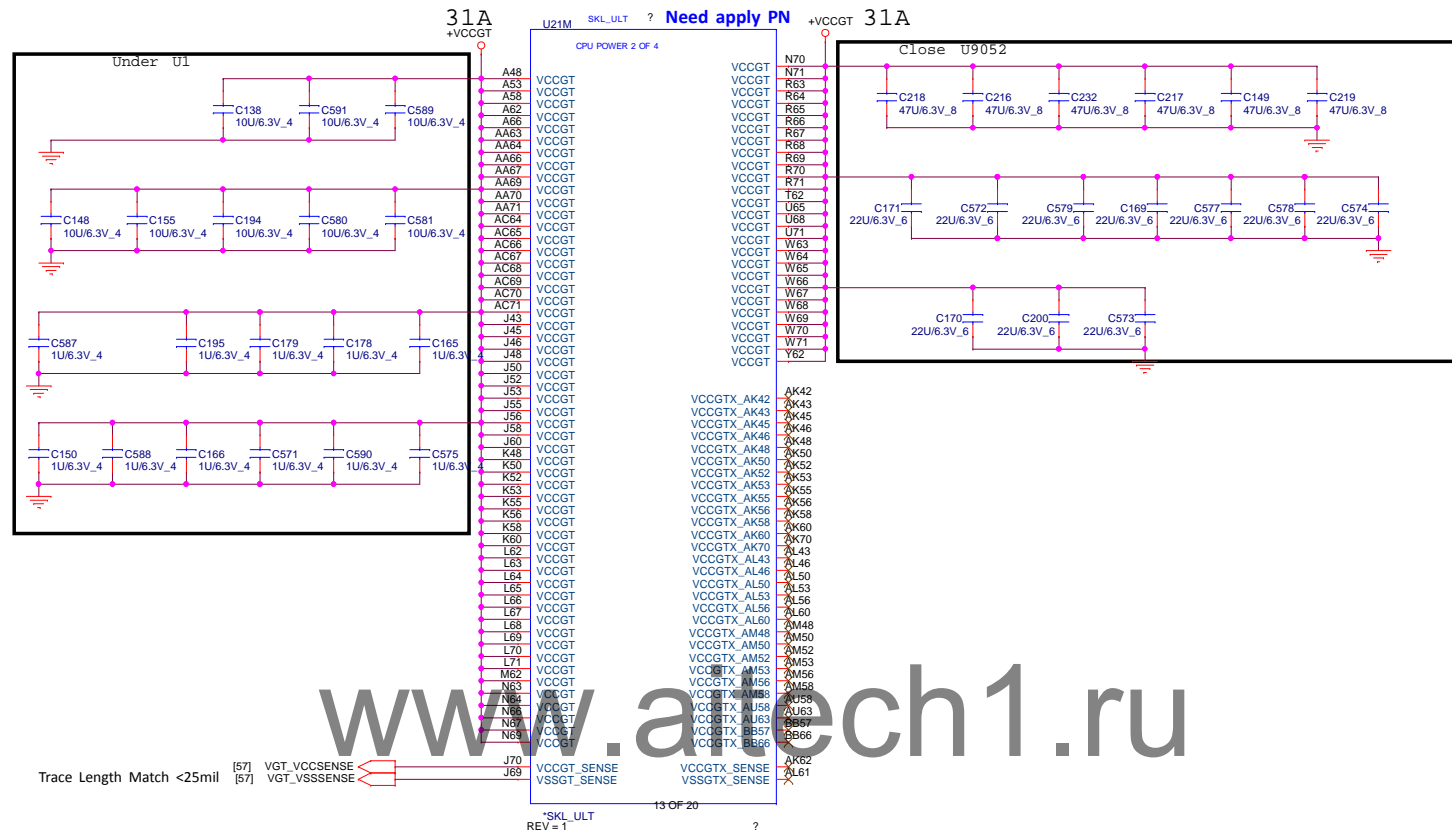


+3V_DEEP_SUS [3,4,5,6,8,37,43,47,48,50,56,59,64]
 +3VPCU [3,33,37,38,40,41,42,44,47,48,49,51,52,53,54,56,59,61,63,64,67]
 +1.0V_DEEP_SUS [9,55,56,59]
 +VCC PRIM
 +3V [2,3,4,5,7,8,9,16,17,18,19,20,24,26,27,29,30,31,33,34,36,38,39,42,43,46,47,48,50,52,57,59,60,64,67]
 +1.8V_DEEP_SUS [3,7,8,9,48,50,55,64]



5	4	3	2	1
---	---	---	---	---

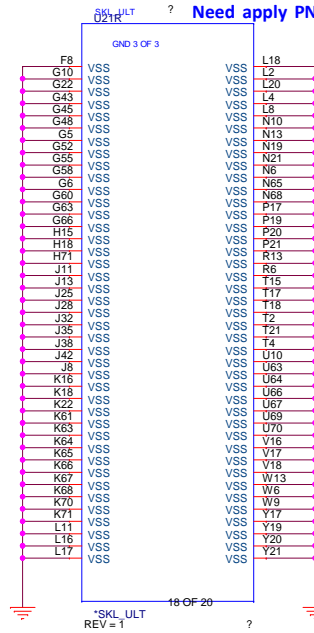
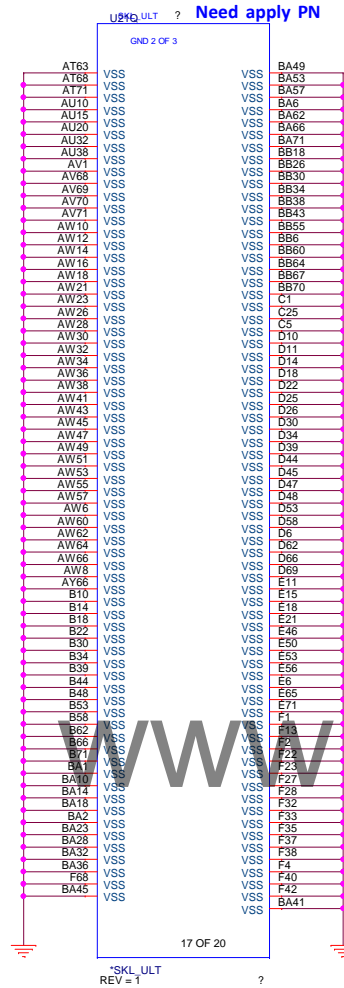
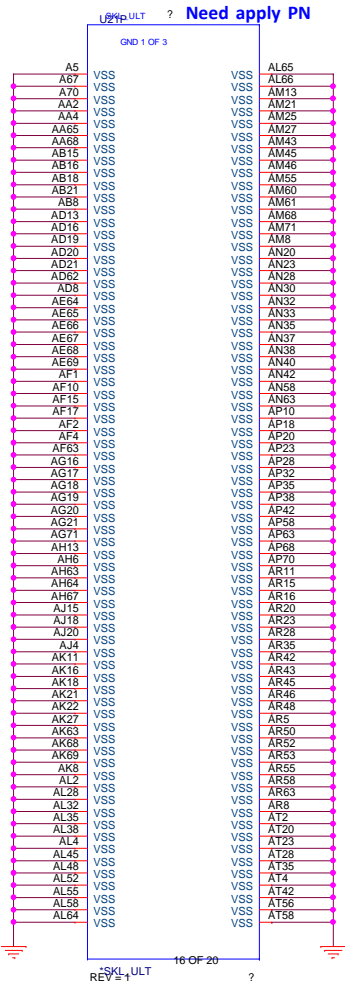




Power Rail	Description	Control
V _{CC}	Processor IA Cores Power Rail	SVID
V _{CCGT}	Processor Graphics Power Rails	SVID
V _{CCGTx}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
V _{CCSA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
V _{CCIO}	IO Power Rail	Fixed
V _{CCST}	Sustain Power Rail	Fixed
V _{CCPLL}	Processor PLLs power rail	Fixed
V _{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
V _{CCOPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V _{CCOPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V _{CCEOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed



Power Rail	Description	Control
V _{CC}	Processor IA Cores Power Rail	SVID
V _{CCGT}	Processor Graphics Power Rails	SVID
V _{CCGTX}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
V _{CCSA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
V _{CCIO}	IO Power Rail	Fixed
V _{CCST}	Sustain Power Rail	Fixed
V _{CCPLL}	Processor PLLs power rail	Fixed
V _{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
V _{CCOPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V _{CCOPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V _{CCEOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed



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10/28 Del XDP

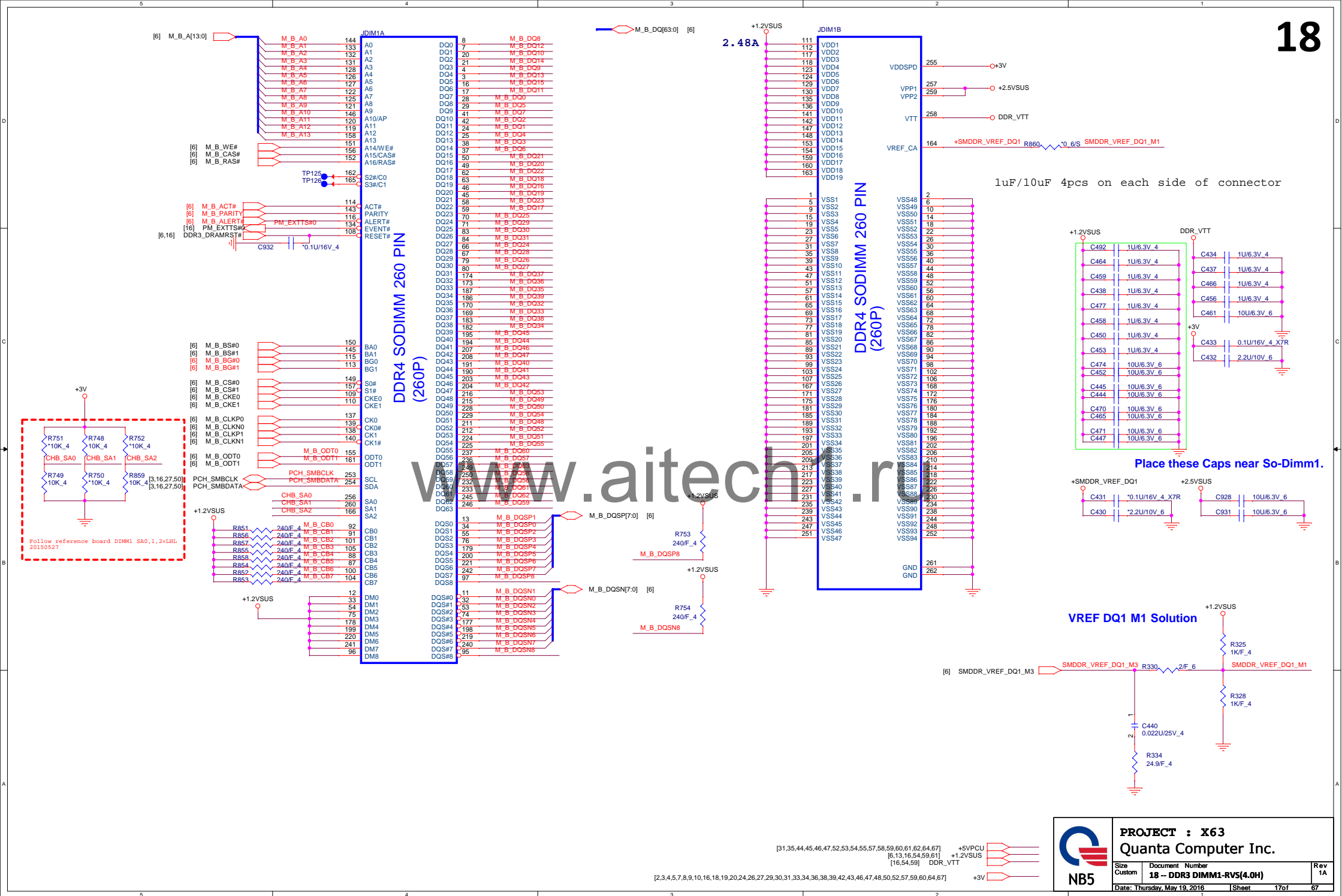
11/03 Del XDP

PV, 0421 Delete APS Connector

11/03 Del XDP

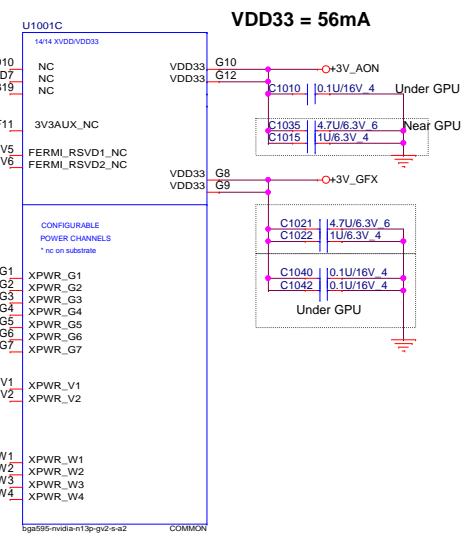
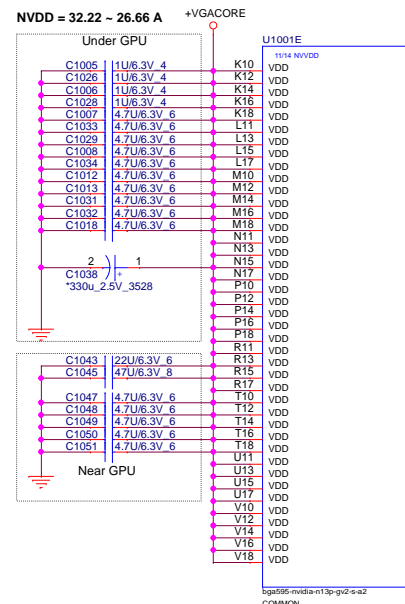
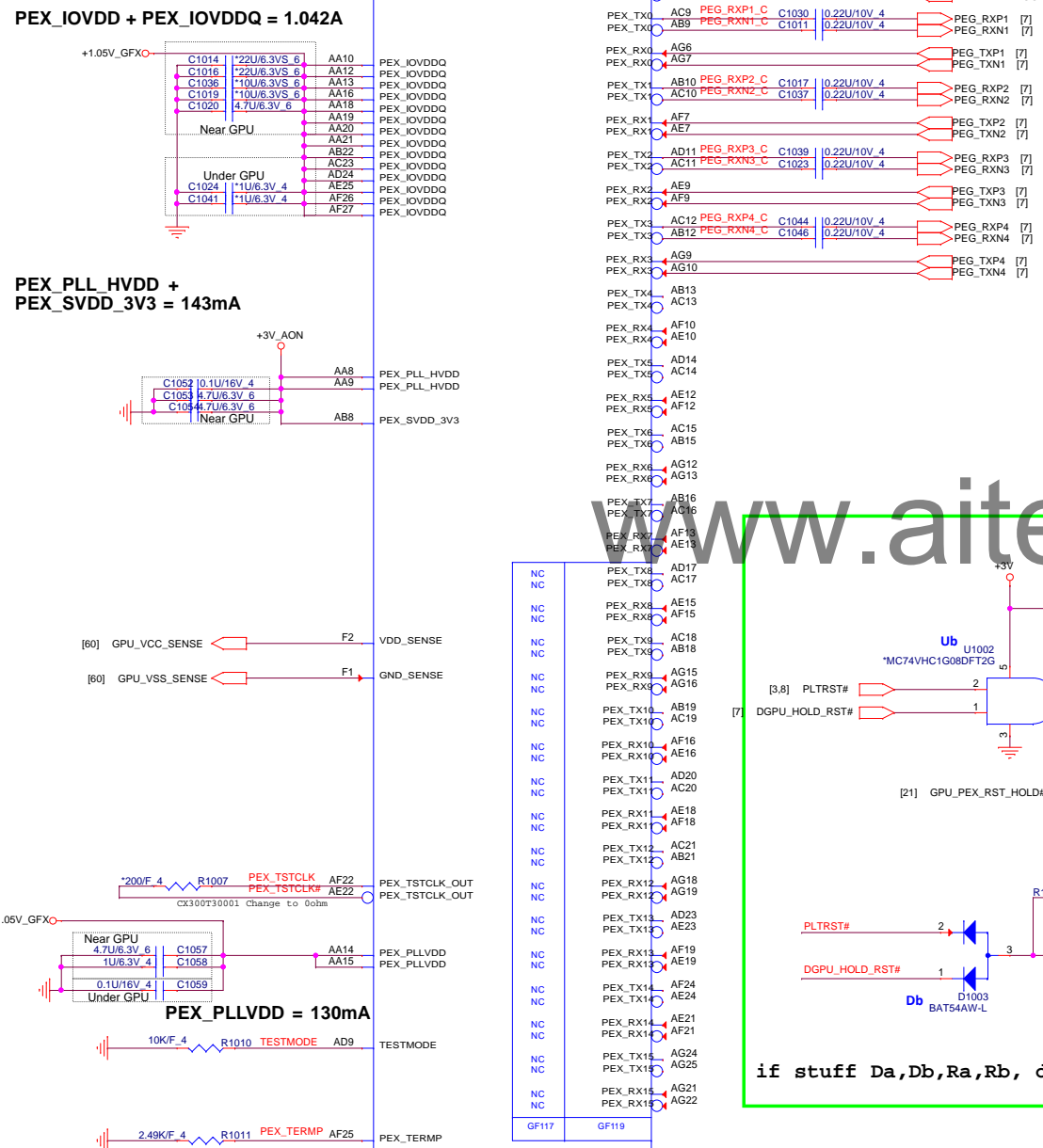
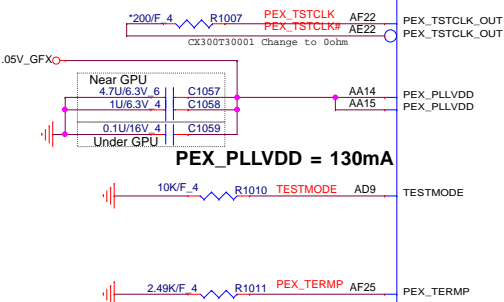
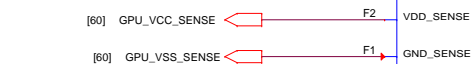
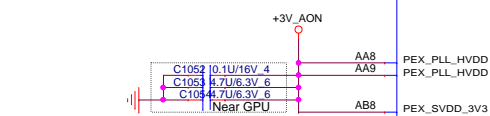
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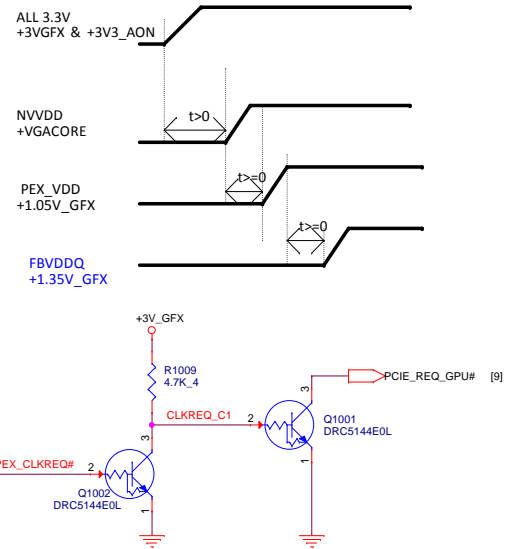


PEX_IOVDD + PEX_IOVDDQ = 1.042A

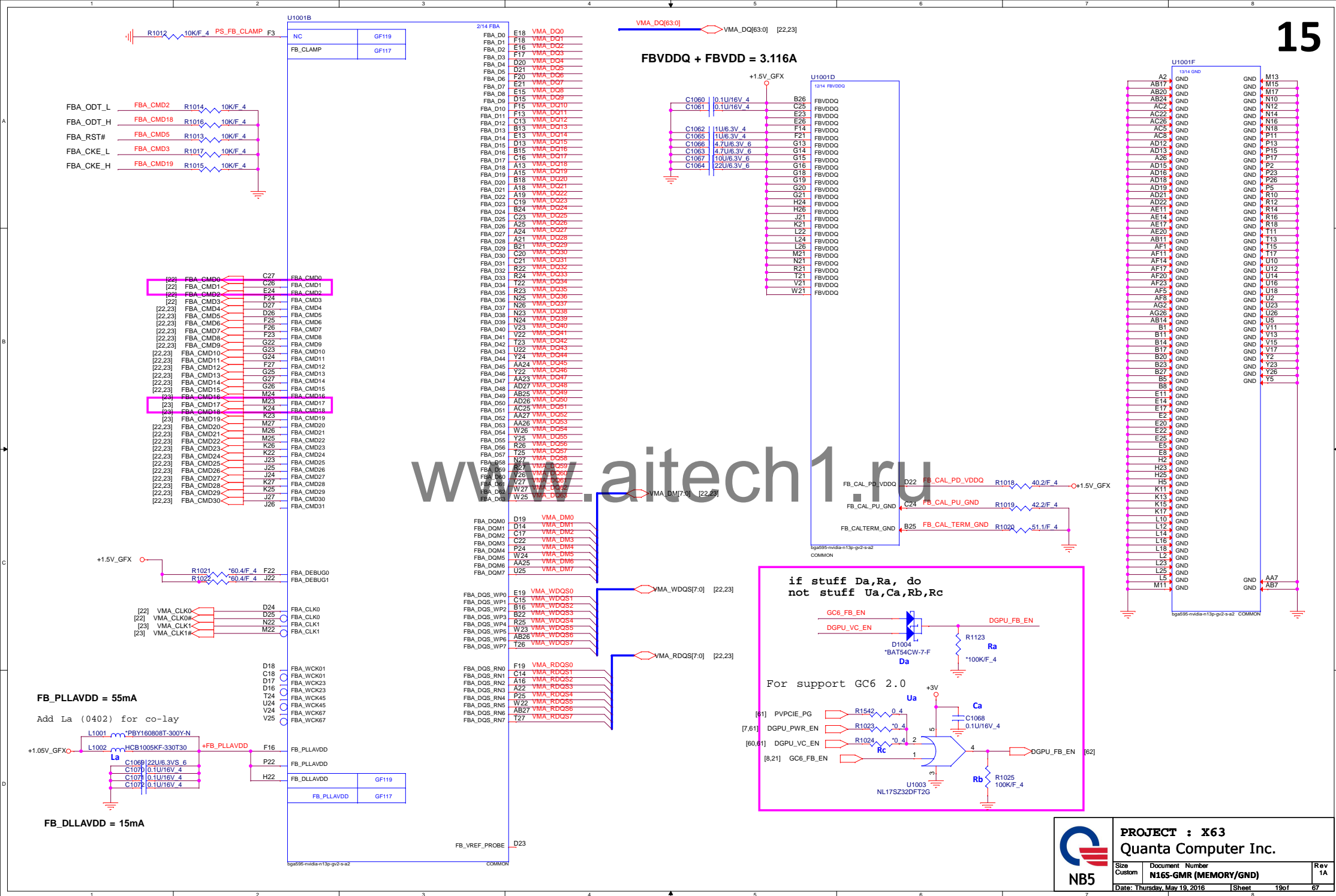
PEX_PLL_HVDD + PEX_SVDD_3V3 = 143mA

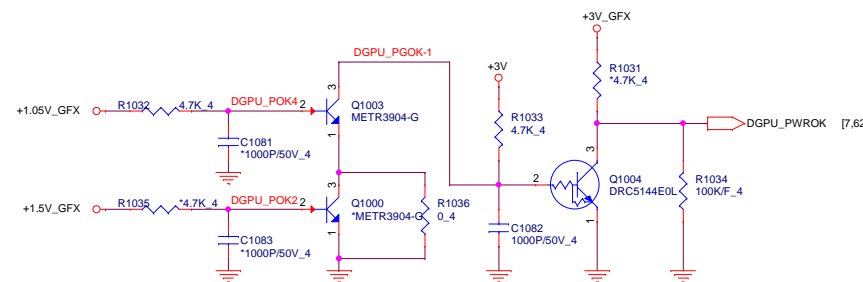
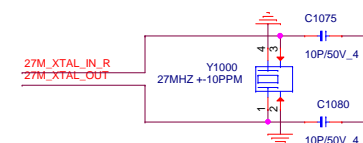
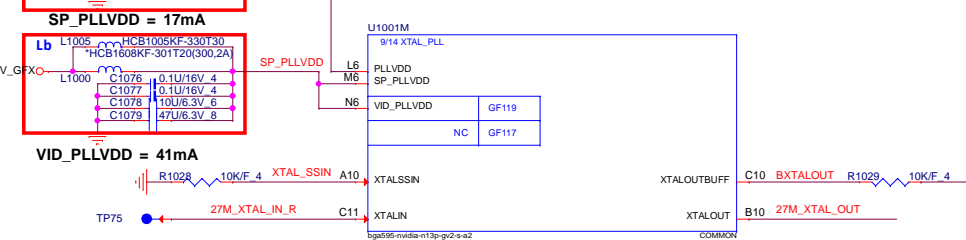
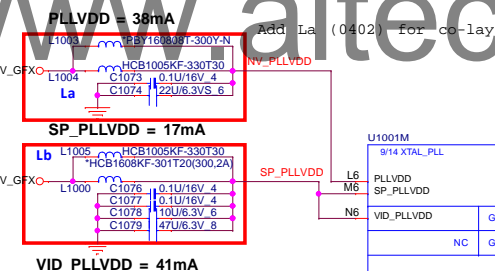
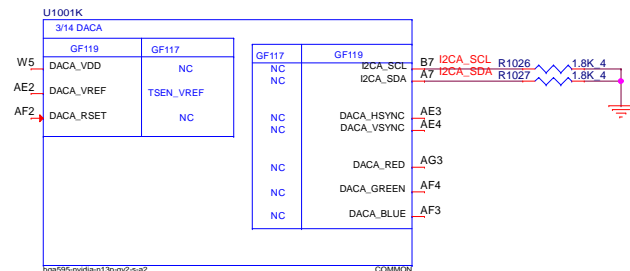
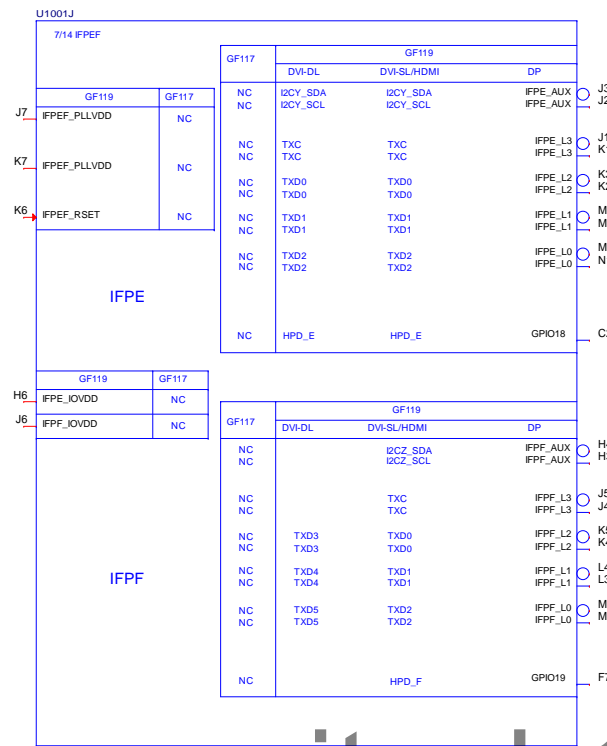


Power up sequence



if stuff Da,Db,Ra,Rb, do not stuff Ua,Ub,Ca,Cb,Rc,Rd





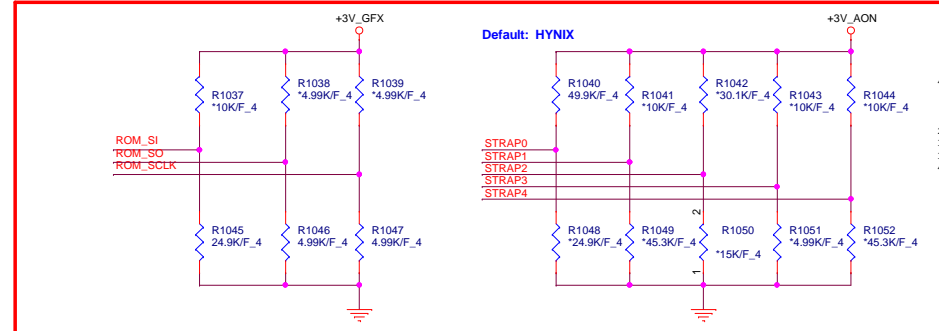
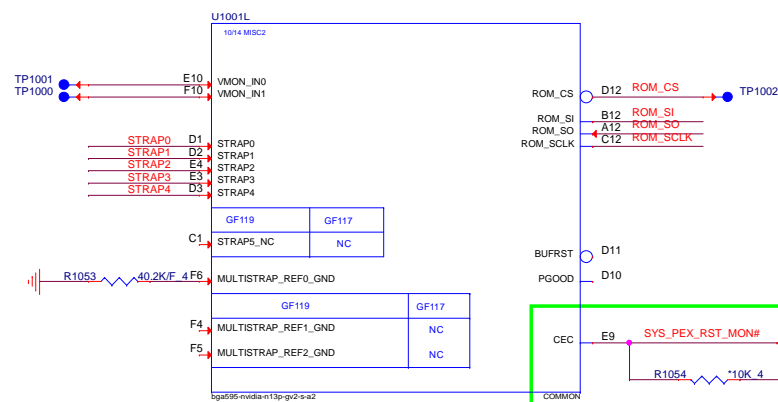
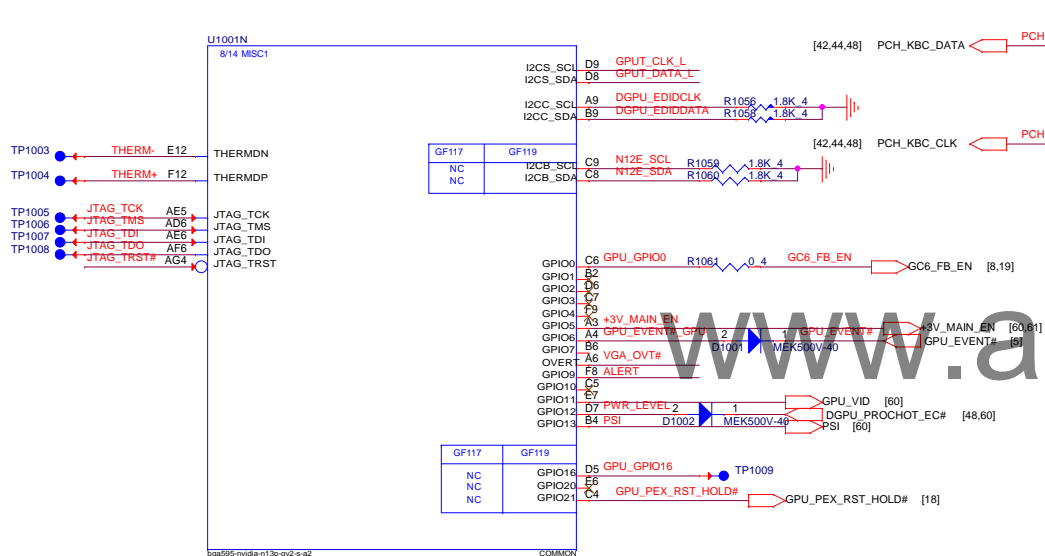


Table 15-2. Resistance Mapping to Hex Values

Resistor Values	Pull-Up to 3V3_MAIN	Pull-Down to GND
4.99 kΩ	1000	0000
10.0 kΩ	1001	0001
15.0 kΩ	1010	0010
20.0 kΩ	1011	0011
24.9 kΩ	1100	0100
30.1 kΩ	1101	0101
34.8 kΩ	1110	0110
45.3 kΩ	1111	0111



VRAM Configuration Table

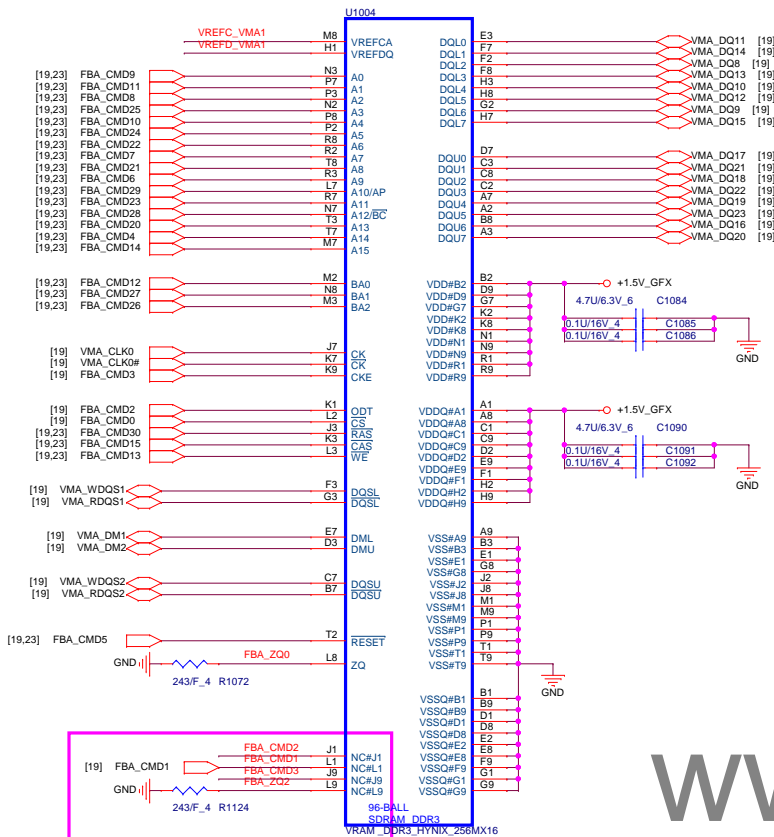
ROM_SI	DESCRIPTION	Vendor	Vendor P/N	Strapping	TOP B/S	QBC
0000	DDR3 - 256Mx16, 1.5V, 1.6Ghz/1.35V 1Ghz	HYNIX	H5TC4G63CFR-N0C	0x5	AKD5PZDTW01	AKD5PZDTW02
0101	DDR3 - 256Mx16, 1.5V, 1.6Ghz/1.35V 1Ghz	Micron	MT41J256M16LY-091G:N	0x3	AKD59G8T11	AKD59G8T10
0100	DDR3 - 256Mx16, 1.5V, 1Ghz/1.35V 900Mhz	SAMSUNG	K4W4G1646E-BC1A	0x4	AKD5PGDT500	AKD5PGDT501

GPIO ASSIGNMENTS

GPIO	I/O	PIN	USAGE
0	IN	FB_CLAMP_MON	FB Clamp monitor
1	OUT	MEM_VDD_CTL	Memory VDD VID
2	OUT	LCD_BL_PWM	Panel Backlight PWM
3	OUT	LCD_VCC	PANEL POWER ENABLE
4	OUT	LCD_BLEN	PANEL BACKLIGHT ENABLE
5	OUT	Reserved	--
6	OUT	FB_CLAMP_TGL_REQ	Active low FB Clamp toggle request
7	OUT	3D VISION	3D VISION LEFT/RIGHT signal
8	I/O	OVERT	ACTIVE LOW THERMAL OVER TEMP
9	I/O	ALERT	ACTIVE LOW THERMAL ALERT
10	OUT	MEM_VREF_CTL	MEMMORY VREF CONTROL
11	OUT	PWR_VID	GPU CORE_VDD PWM Control signal
12	IN	PWR_LEVEL	AC Power detect or power supply overdraw input
13	OUT	PSI	Phase Shedding

Rank0

HYU 256Mx16, H5TC4663AFR-11C QBC PN AKD5PGWTW08---TOP B/S PN : AKD5PGWTW07
 MIC 256Mx16, MT41J256M16HA-093G:E QBC PN AKD5PZSTL01---TOP B/S PN : AKD5PZSTL00
 SAM 256Mx16, K4W4G1646D-BC1A QBC PN AKD5PGWT501---TOP B/S PN : AKD5PGWT502



stuff R1124 for
Hynix 8Gb DDP VRAM

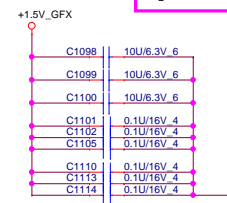
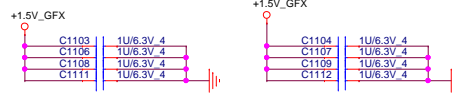
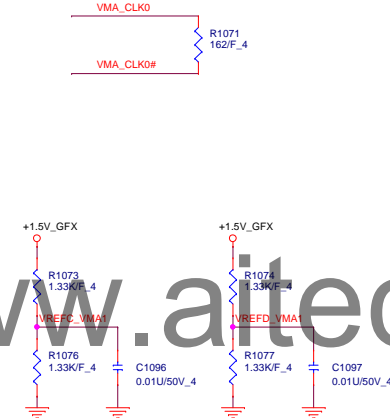
reserve for Hynix 8Gb DDP VRAM

SDDR3_BGA100

	0..31	32..63
CMD0	CS0*	
CMD1	CS1*	
CMD2	ODT	
CMD3	CKE	
CMD16		CS0*
CMD17		CS1*
CMD18		ODT
CMD19		CKE

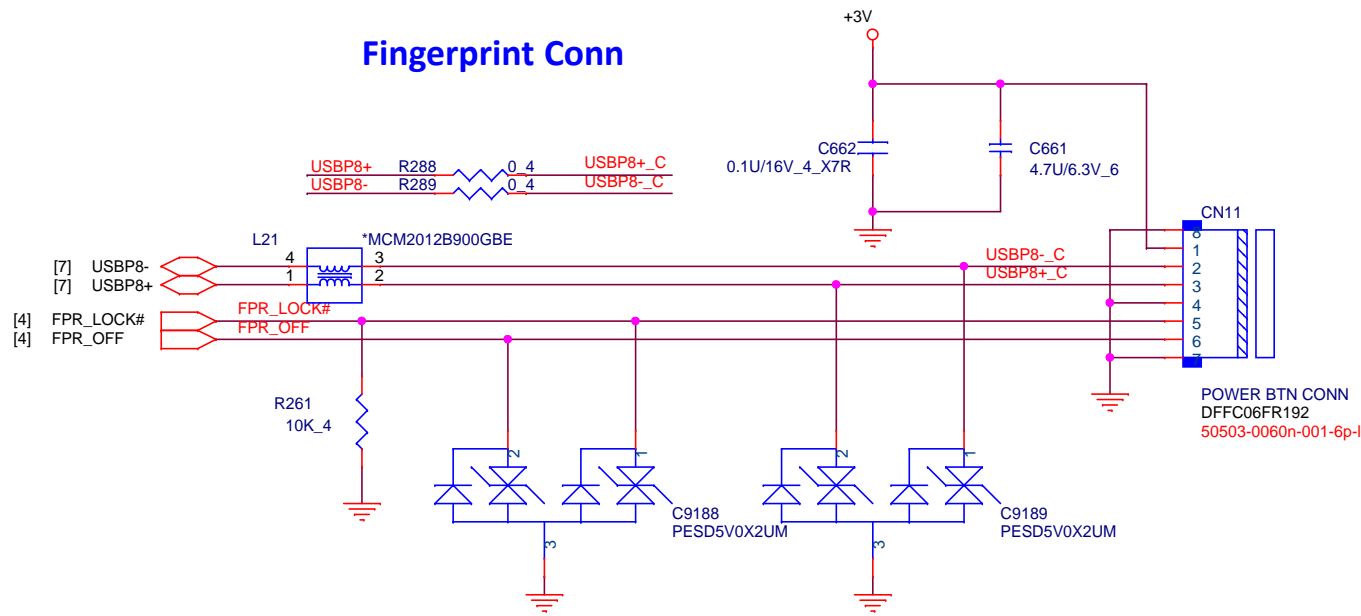
SNN FBAO ODT1	J1	NC/ODT1
SNN FBAO CKE1	J9	NC/CKE1
SNN FBAO CS1	L1	NC/CS1
SNN FBAO ZQ1	L9	NC/ZQ1

162_1% ohm CS11622FB07 RES CHIP 162 1/16W +-1%(0402)
 CS11622FB15 RES CHIP 162 1/16W +-1%(0402)



stuff R1125 for
Hynix 8Gb DDP VRAM

Fingerprint Conn



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ALF@1119:
HP confir med to re move the eDP to LVDS convert α.

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[2,3,4,5,7,8,9,10,16,17,18,19,20,24,26,27,29,30,31,33,34,36,38,39,42,43,46,47,48,50,52,57,59,60,64,67]

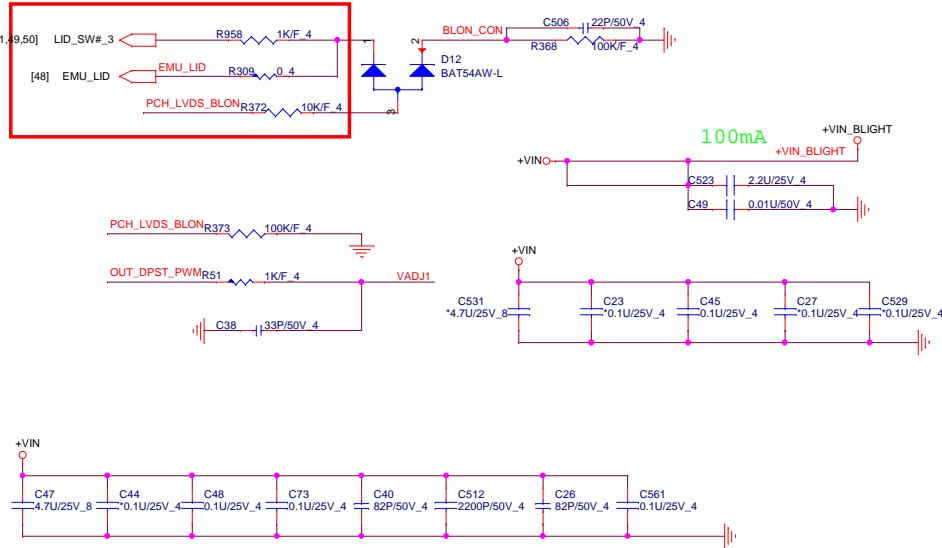
+3V



 NB5	PROJECT : X63		
	Quanta Computer Inc.		
	Size Custom	Document Number 25 -- LVDS converter RTD2136	Rev 1A
Date: Thursday, May 19, 2016 Sheet 25 of 67			

LID Switch

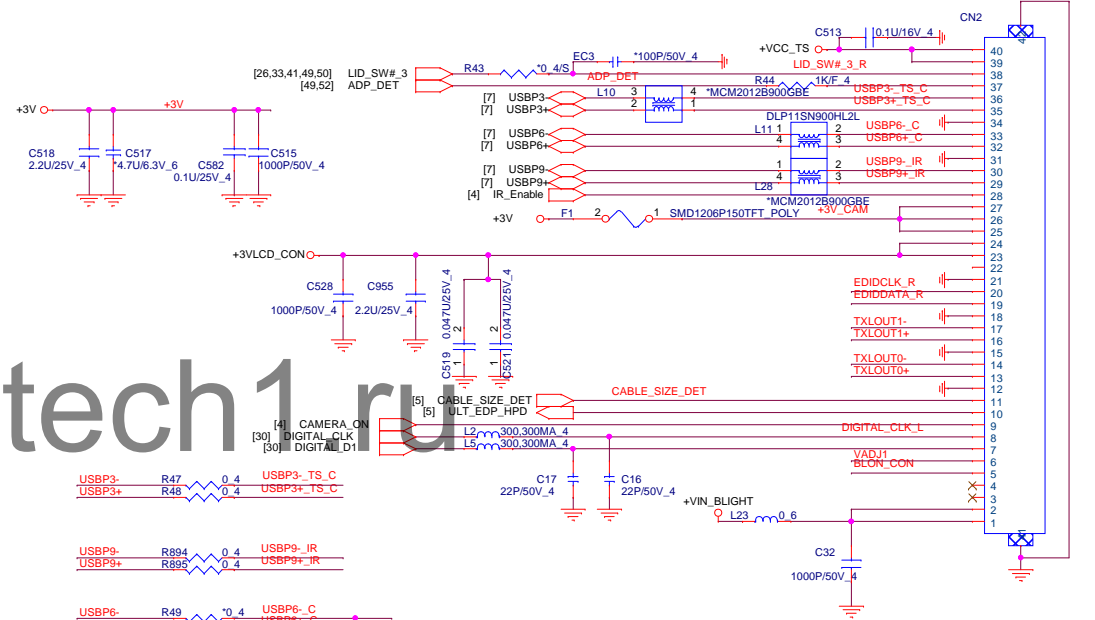
26



LVDS Conn.

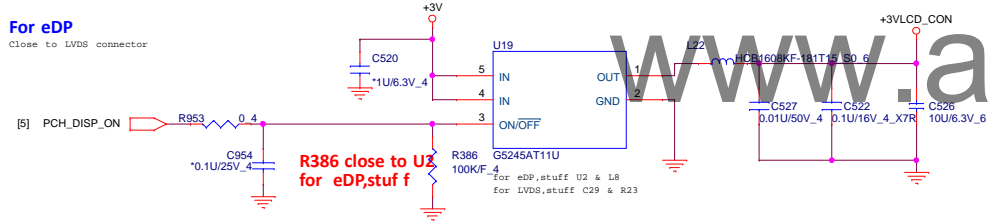
GS12401-1011-9H
51519-04001-v02-40p-I

DFFC40FR081

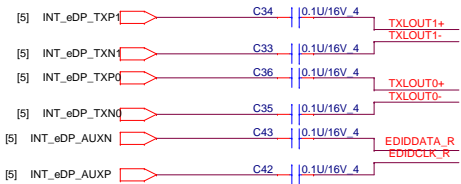


For eDP

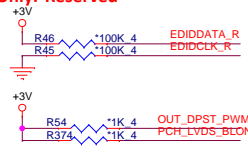
Close to LVDS connector



For EDP Only: stuff Cap For LVDS only stuff Resistor



For EDP Only: Reserved



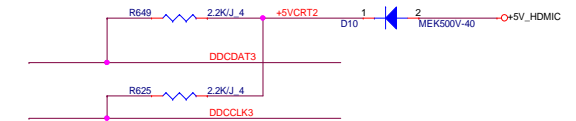
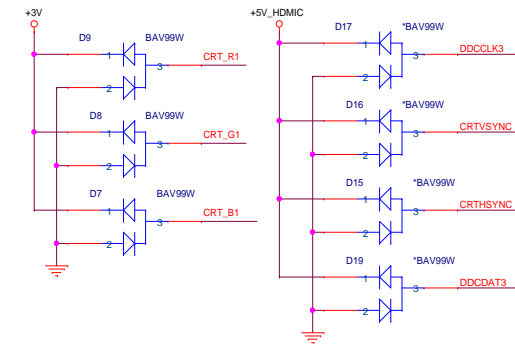
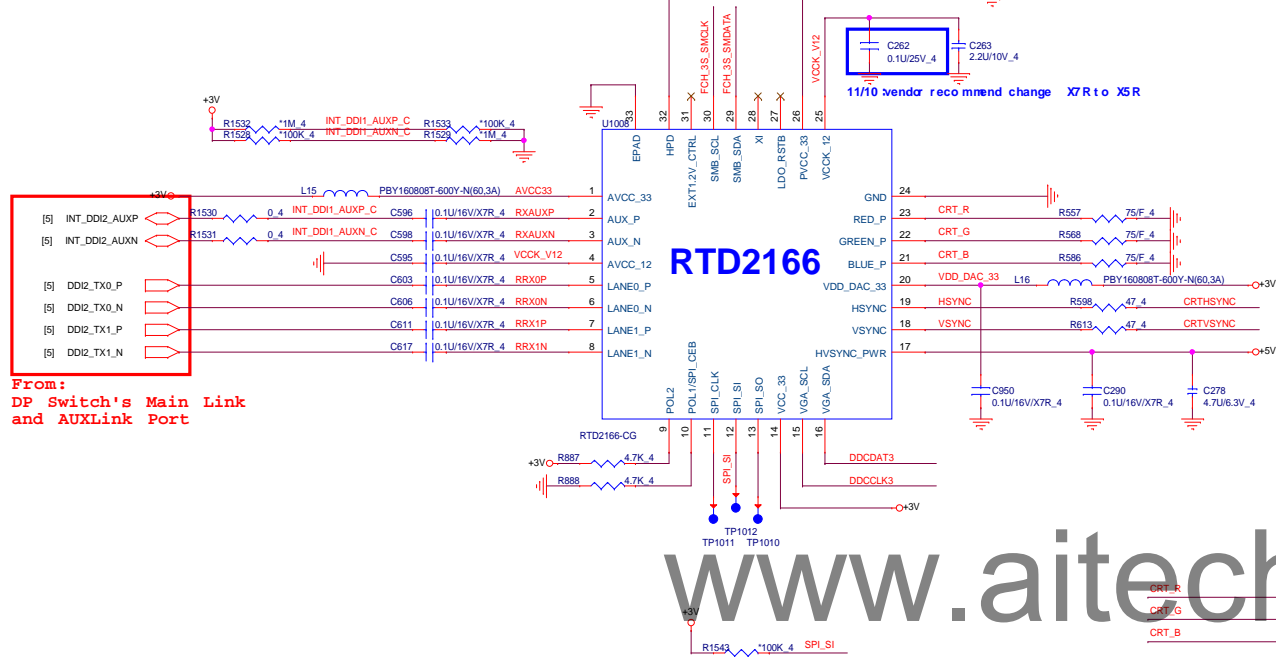
For eDP, close to CN2



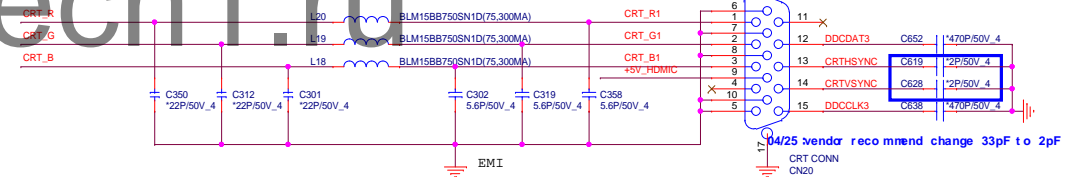
PROJECT : X63
Quanta Computer Inc.

Size	Document Number	Rev
Custom	26 -- LCD CONN/LID/CAM/D-MIC	1A
Date: Thursday, May 19, 2016	Sheet 26 of 67	

To:
DP Switch's HPD Input Port
[5] DDI_HPD_CON
Pull down at SOC side



40 MIL
C676 0.1u/16V 4 X7R
SSM14 spec is 40V 1A



Need check footprint and PN

DFDS15FR456
dsu-10556-15002-15p

FCH_3S_SMCLK, FCH_3S_SMDATA Connection

EP mode: Pin2, Pin3 connect to EC SMBUS
ROM or EEPROM mode: connect to PCH SMBUS
IIC Protocol is used

RTD2168 Slave Address:
0x64/0x65 and 0x68/0x69

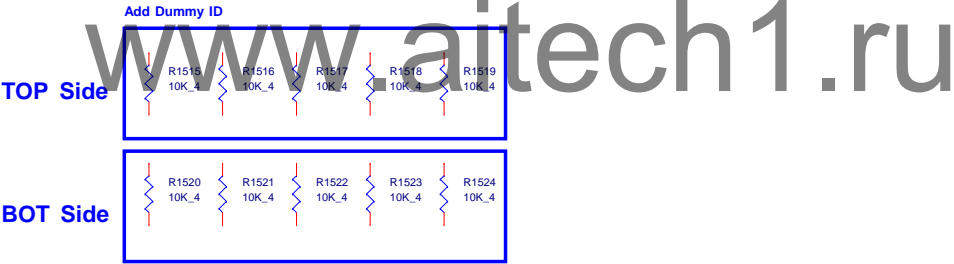
From PCH




PROJECT : X63
Quanta Computer Inc.

Size Custom	Document Number 27 - DP2VGA_converter	Rev 1A
Date: Thursday, May 19, 2016	Sheet 27 of 67	

Inputs		Equalization for 3 Gbit/s
EQ1	EQ0	
short to GND	short to GND	0 dB
short to GND	short to V _{DD}	2 dB
short to V _{DD}	short to GND	4 dB
short to V _{DD}	short to V _{DD}	6 dB



OE_N	DDC_EN	HPD_SINK	Source output	PTN3366 power mode
LOW	HIGH	HIGH	source active	Active mode; DDC active
LOW	LOW	LOW	don't care	Standby mode
HIGH	LOW	don't care	don't care	Ultra low-power mode



PROJECT : X63

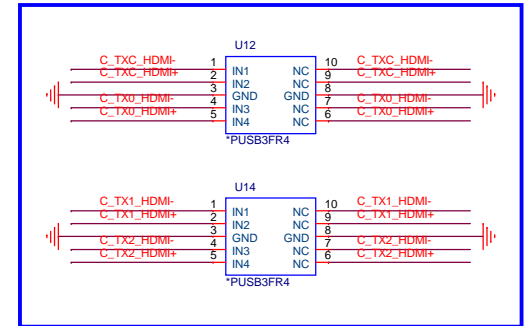
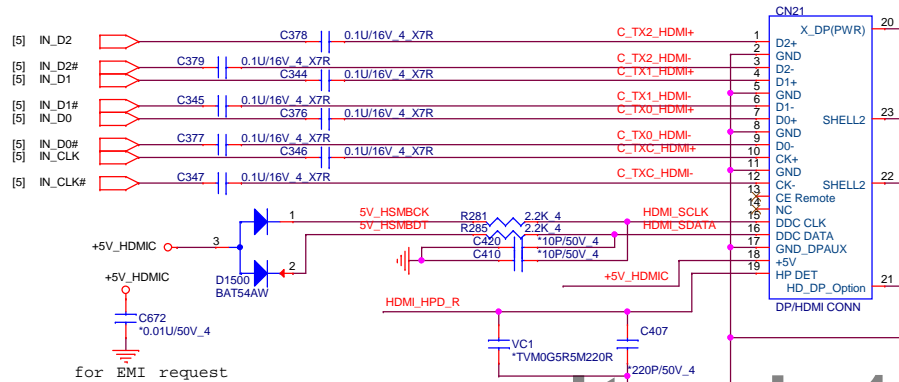
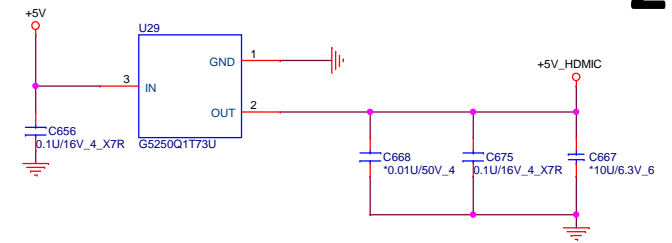
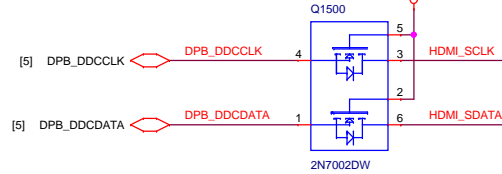
Quanta Computer Inc.

Size Custom	Document Number	Rev 1A
28 – REPEATER PTN3366		
Date: Thursday, May 19, 2016	Sheet 28 of 67	

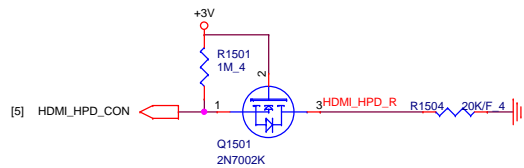
EMI Solut i on

C_TX2_HDMI+	R304	150/F 4	C_TX2_HDMI-
C_TX1_HDMI+	R291	150/F 4	C_TX1_HDMI-
C_TX0_HDMI+	R295	150/F 4	C_TX0_HDMI-
C_TXC_HDMI+	R299	150/F 4	C_TXC_HDMI-

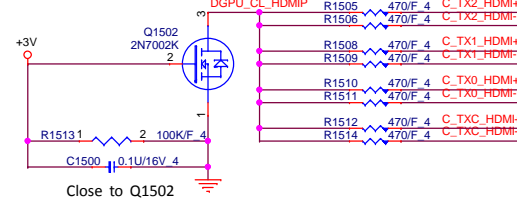
HDMI SMBus Isolati on



www.aitech1.ru



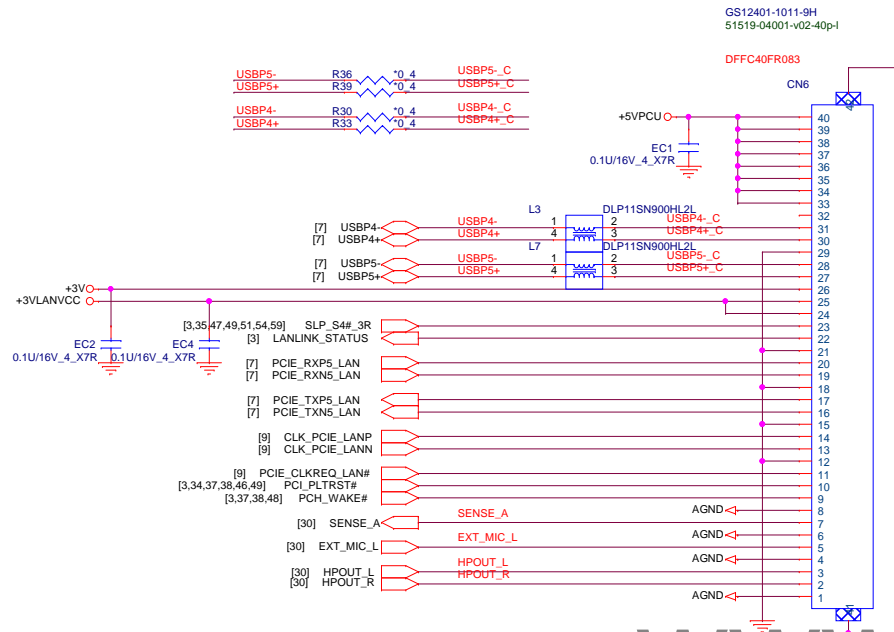
Close to HDMI connector



PROJECT : X63
Quanta Computer Inc.

Size Custom	Document Number 29 -- HDMI CONNECTOR	Rev 1A
Date: Thursday, May 19, 2016	Sheet 29 of 67	

USB2.0 x2/LAN/Headphone_Mic Combo Jack Daugther Board Connector



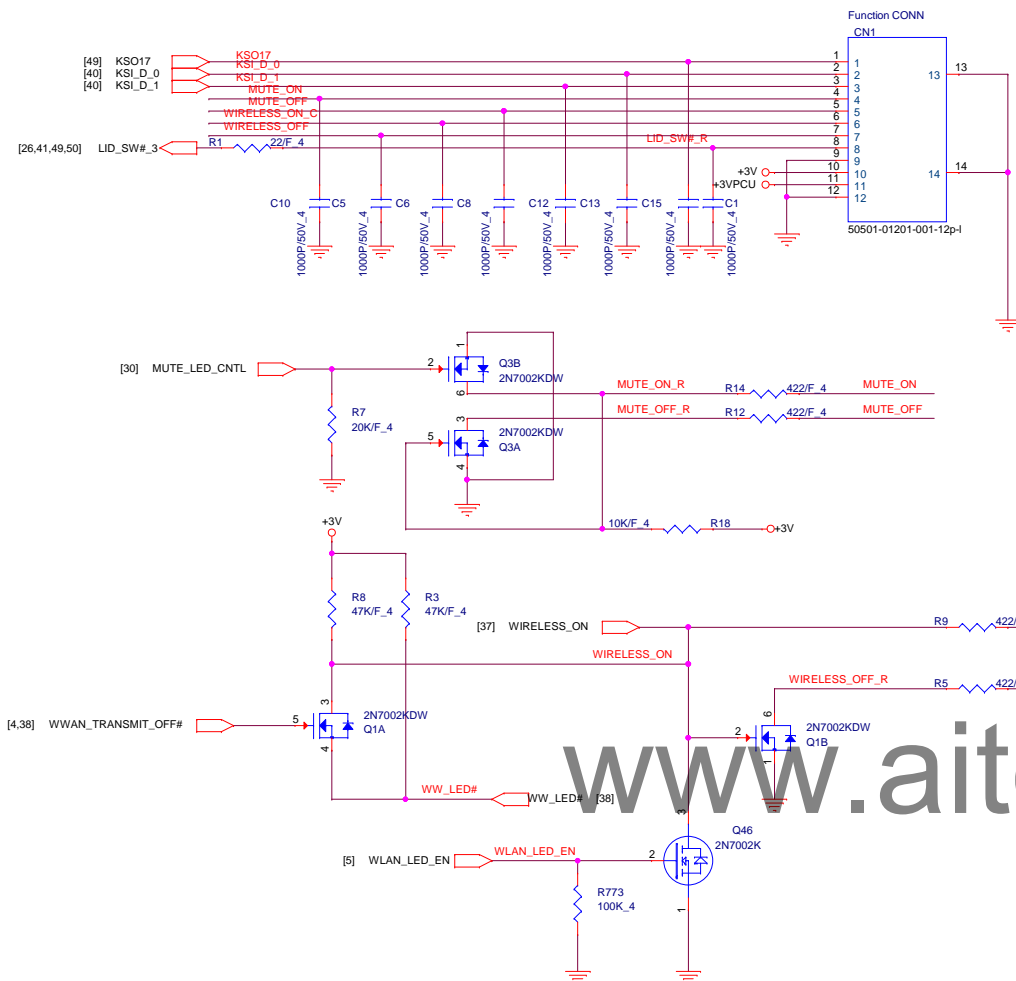
www.aitech1.ru



PROJECT : X63
Quanta Computer Inc.

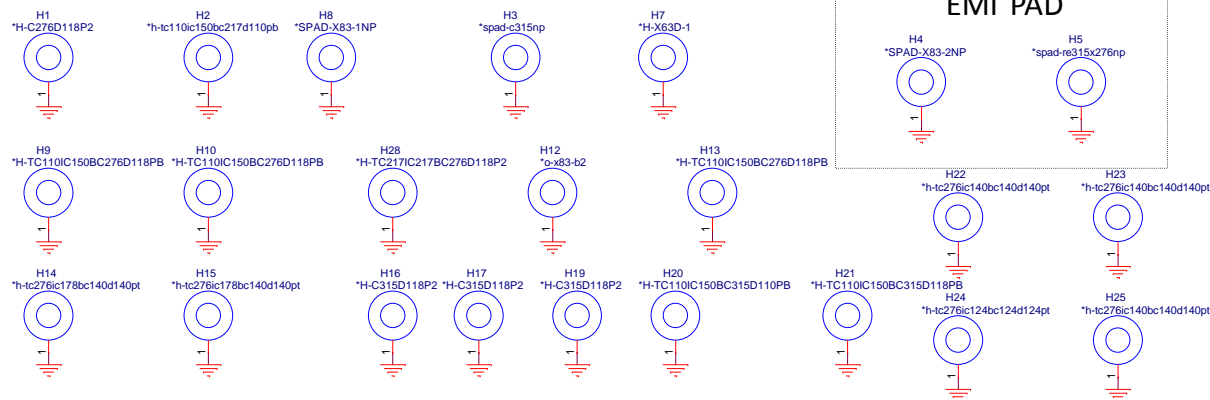
Size Custom	Document Number 31 -- DAUGHTER BOARD CONN.	Rev 1A
Date: Thursday, May 19, 2016		Sheet 31 of 67

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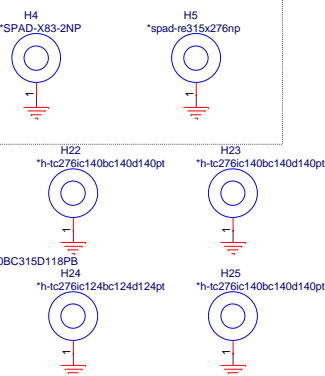


www.aitech1.ru

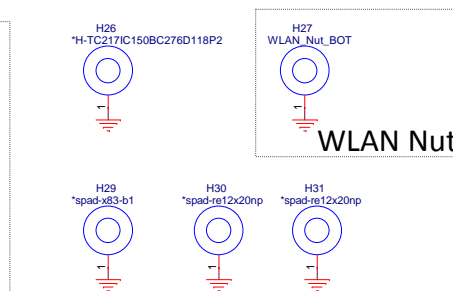
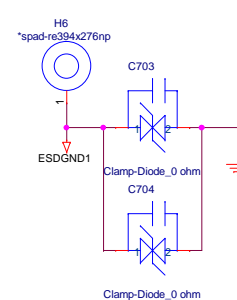
Hole

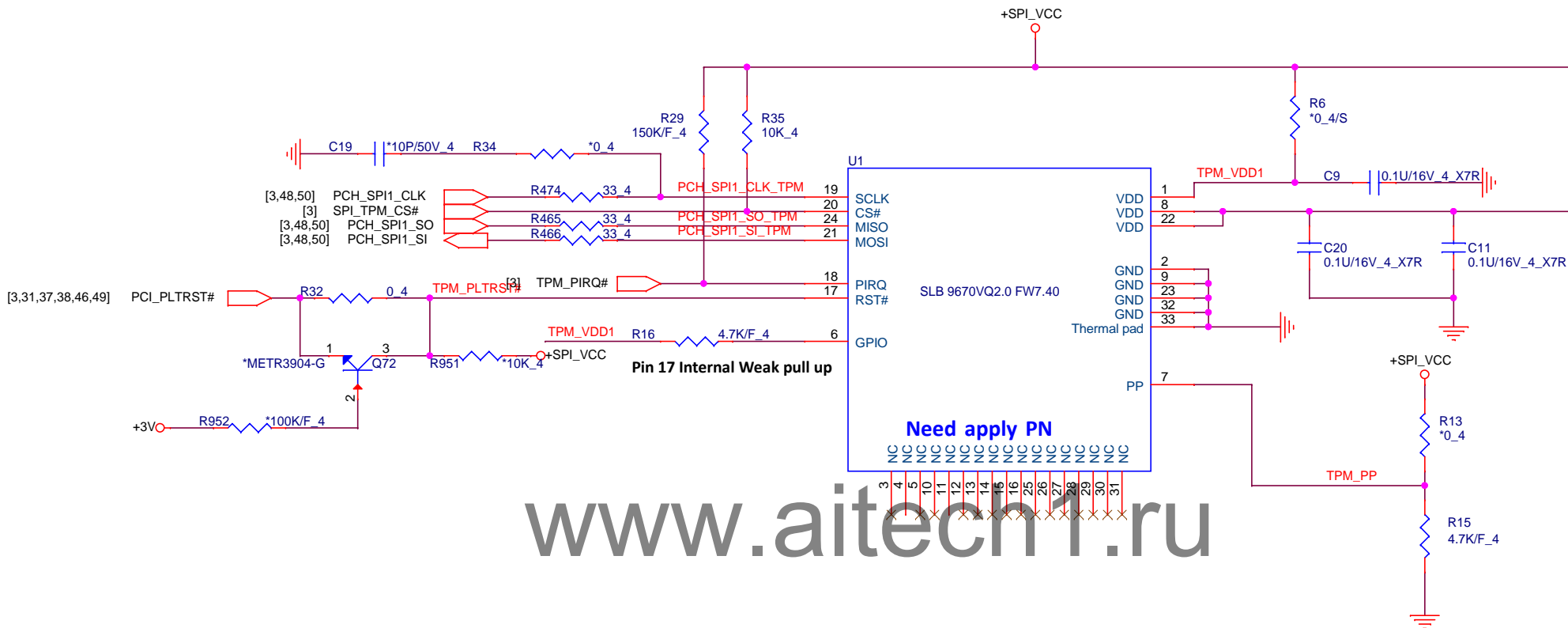


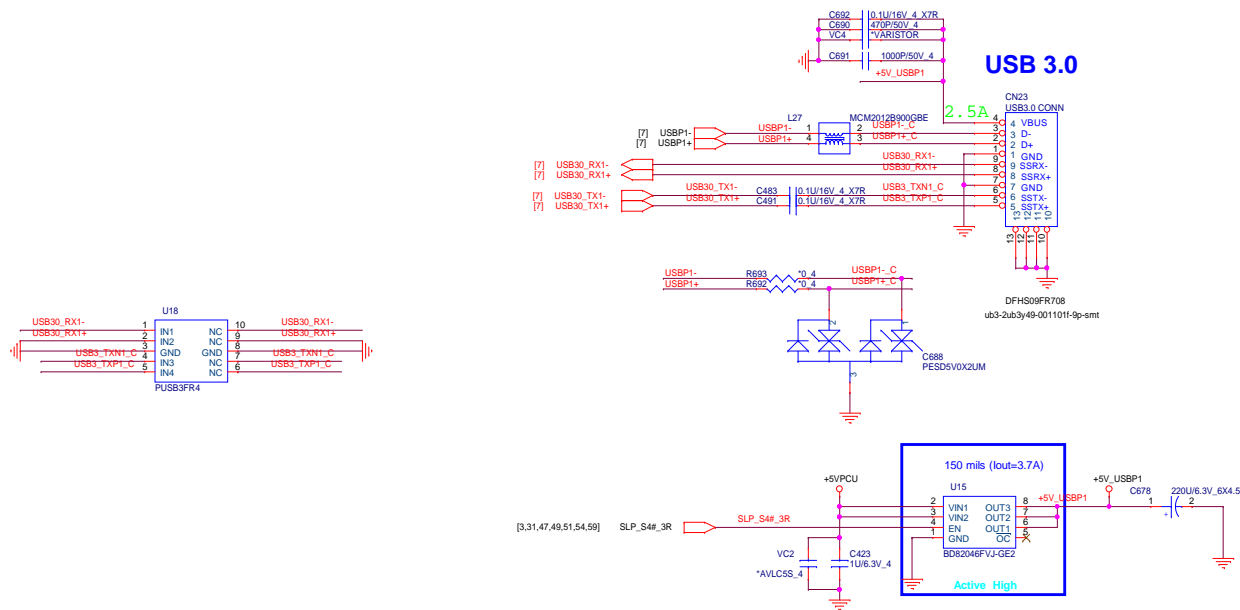
EMI PAD



ESD PAD







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[31,44,45,46,47,52,53,54,55,57,58,59,60,61,62,64,67]
[9,41,51,52,53,59,63,64,67]

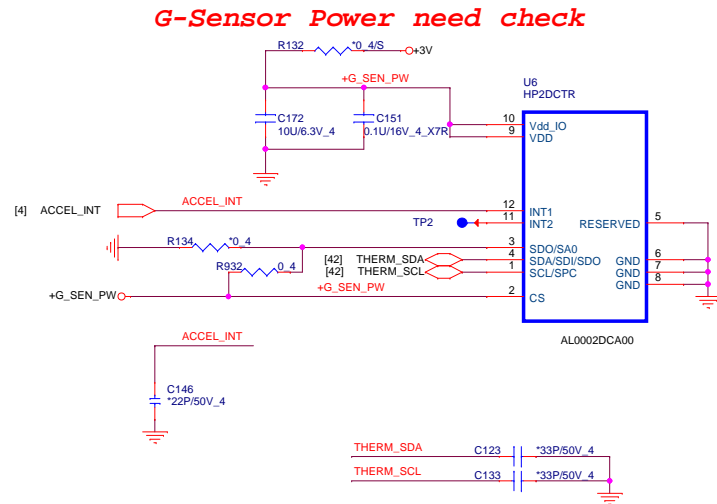
+5V_PCU
+3V_ALW



PROJECT : X63
Quanta Computer Inc.

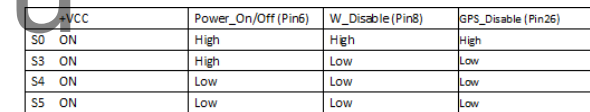
Size Custom	Document Number 35 -- USB3.0 x2	Rev 1A
Date: Thursday, Mar 19, 2016		Sheet 35 of 67

Accelerometer Sensor

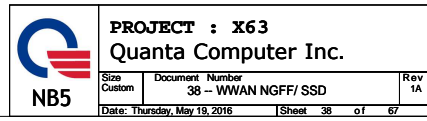


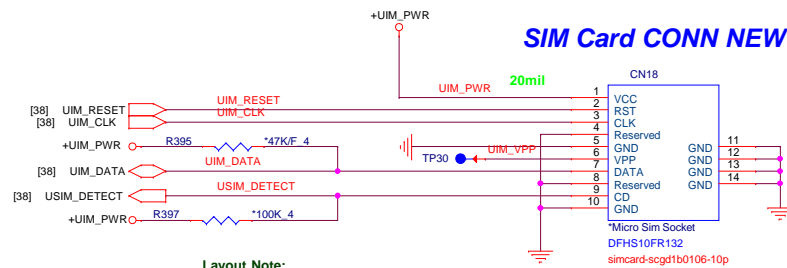
www.aitech1.ru

[31,35,44,45,46,47,52,53,54,55,57,58,59,60,61,62,64,67] +5VPCU
[9,41,51,52,53,59,63,64,67] +3V_ALW

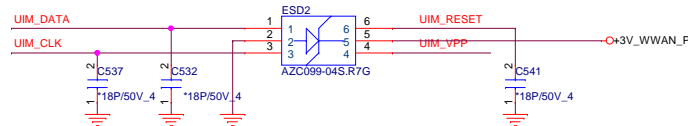
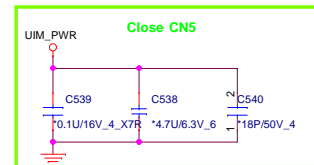


↰	M.2 Pinout ↰	S0 ↰	S3 – S5 ↰
WWAN 3.3V	2, 4, 70, 72, 74	On	Off



**Layout Note:**

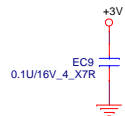
1. UIM_RESET, UIM_CLK, UIM_DATA routing as short as possible. Route into ESD then go out.
2. Avoid routing the SIM_CLK and SIM_DATA lines in parallel over distances ≥ 2 cm.
3. Position the SIM connector from the WWAN module ≤ 100 mm if possible, NOT exceed length is 150mm.

**Trace Length and Routing**

- Special attention should be paid to SIM traces (UIM_CLK, UIM_DATA and UIM_RST) to minimize the trace lengths between the SIM slot and the WWAN NGFF slot. **Minimizing the signal lengths and traces will reduce possibility of SIM signal integrity issues.** Recommended maximum length is 100mm. Not to exceed length is 150mm.
- Minimum distance between UIM_CLK and UIM_DATA should be 20 mils. Static signals such as UIM_RST can be routed between UIM_CLK and UIM_DATA to conserve space if needed.
- It is recommended that SIM traces be isolated from other high-speed switching signals, as noise can couple into the SIM signals. Keep a minimum distance of 20 mils between UIM_CLK, UIM_DATA and any other high-speed switching signals.
- Placing the SIM card on a daughter card is also not recommended as the interconnect may impact SIM signal integrity.

SIM Power

- The UIM_PWR trace width must be at least 20 mils. Sub-planar routing is recommended.
- Implement additional power filtering to SIM card power to ensure clean power is supplied to minimize any possible noise ripple effects. At a minimum, place a 0.1uF and a 4.7uF capacitor on the UIM_PWR supply and locate near the SIM connector.



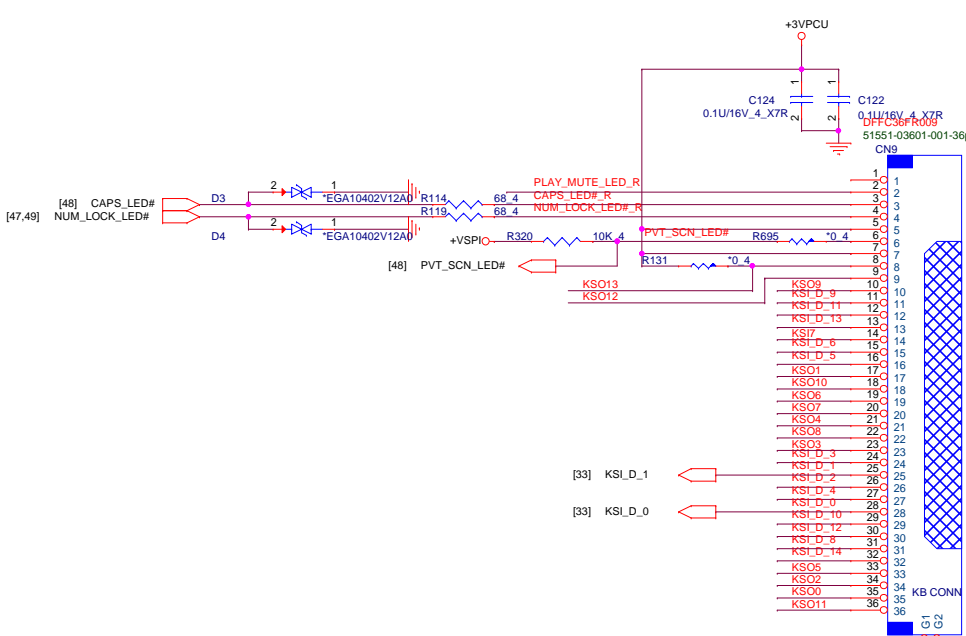
www.aitech1.ru



PROJECT : X63
Quanta Computer Inc.

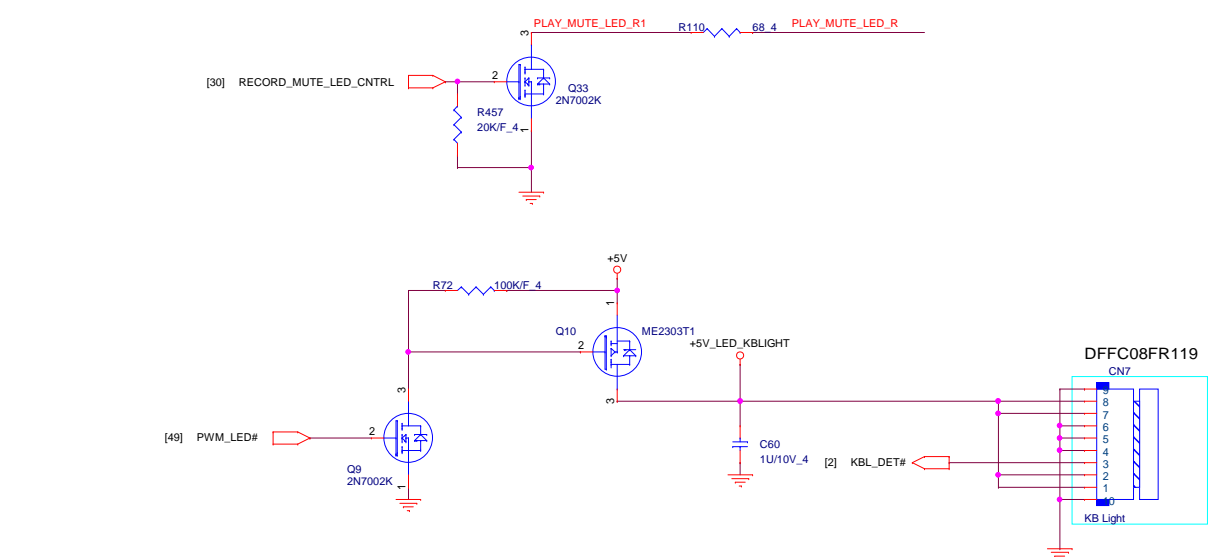
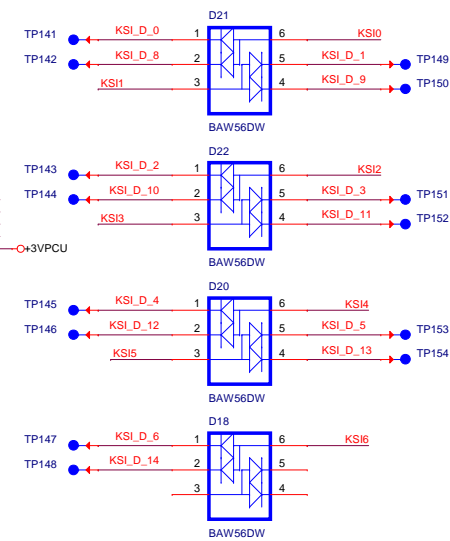
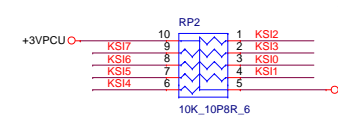
Size Custom	Document Number 39 -- SIM CARD/ RF cap	Rev 1A
Date: Thursday, May 19, 2016	Sheet 39 of 67	

KEYBOARD Con.

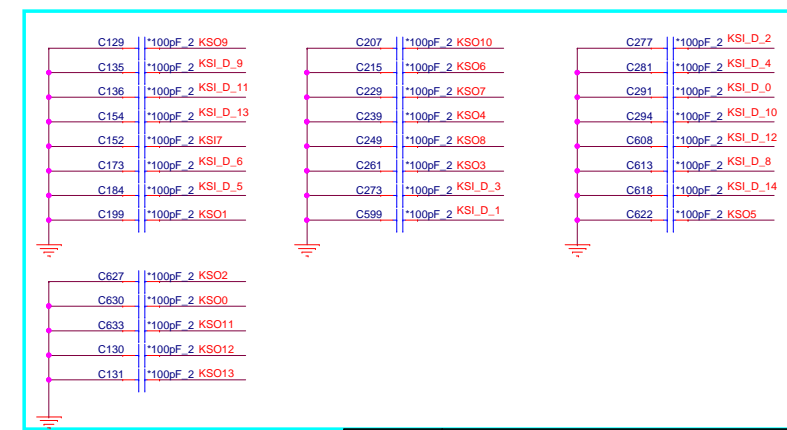


Need apply PN & FOOTPRINT

KEYBOARD PULL-UP



For EMI reserved



[2,3,4,5,7,8,9,10,16,17,18,19,20,24,26,27,29,30,31,33,34,36,38,39,42,43,46,47,48,50,52,57,59,60,64,67]

[8,27,29,30,42,43,55,59,64,67]

[9,41,51,52,53,59,63,64,67]

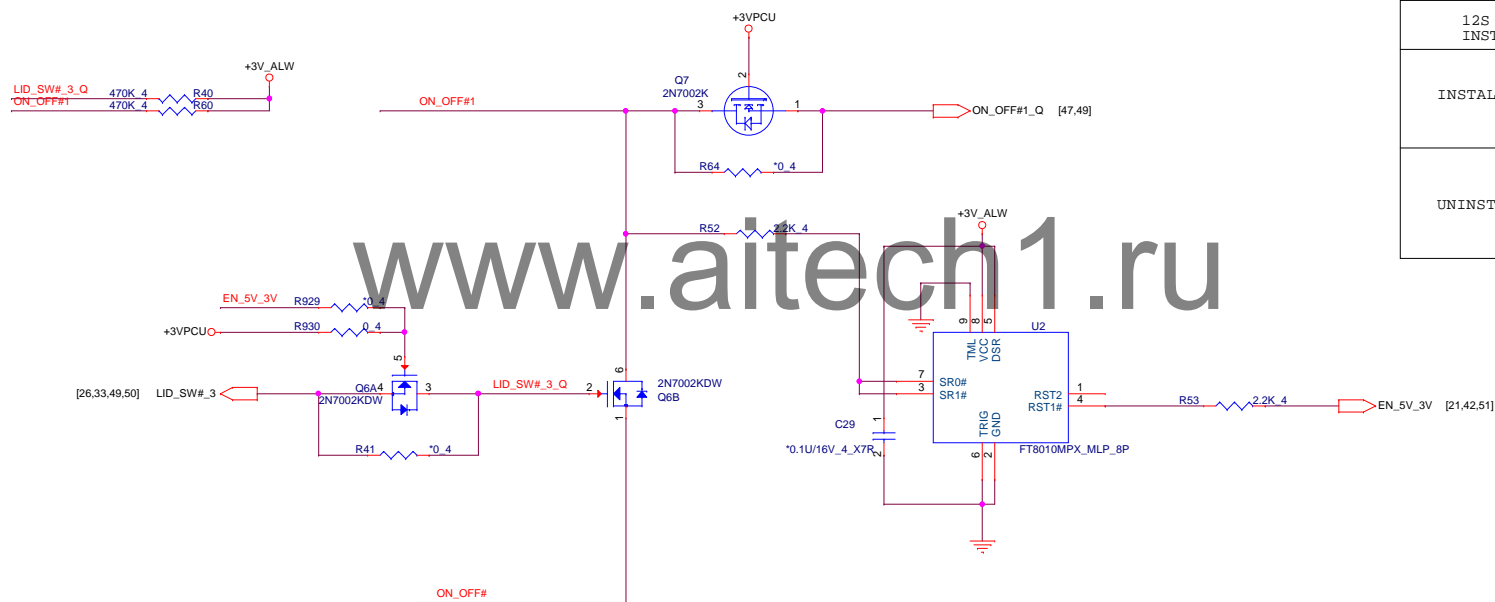
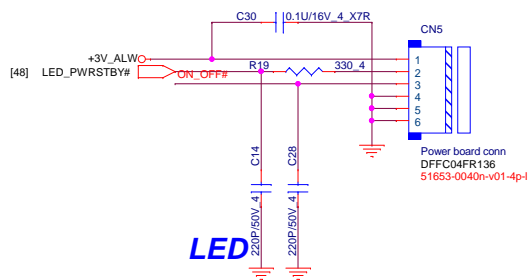
3+V

5+V

3+V_ALW

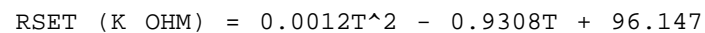
PROJECT : X63
Quanta Computer Inc.

Size Custom	Document 40 -- KB/ KB light CONN	Number 1A
Date: Thursday, May 19, 2016	Sheet 40 of 67	Rev 1A

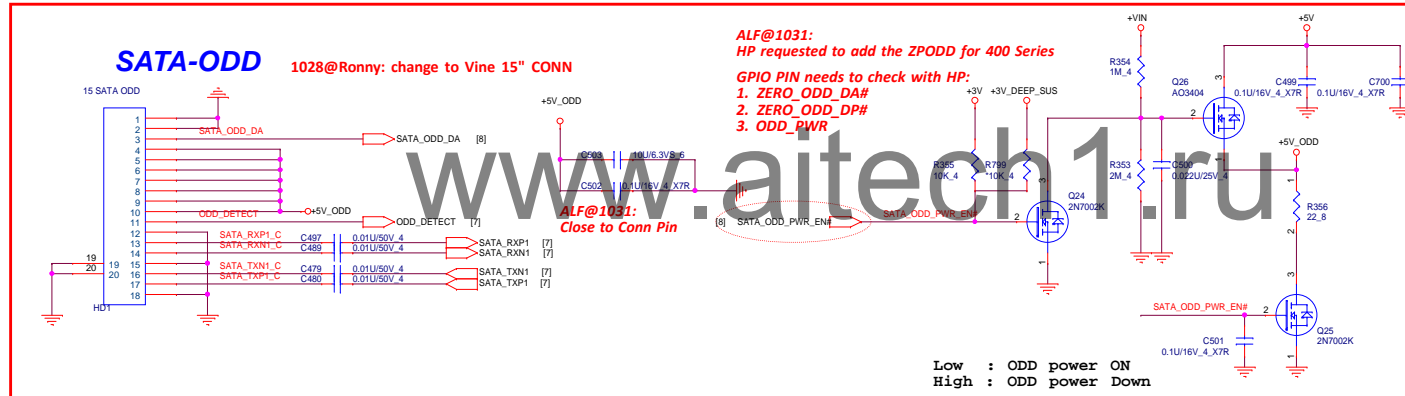
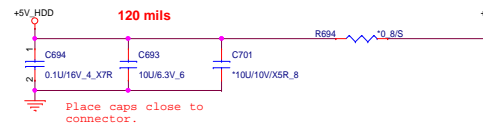
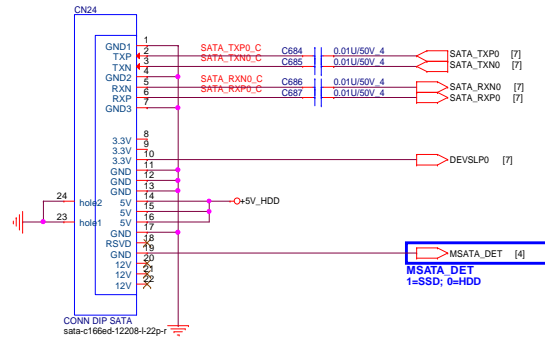


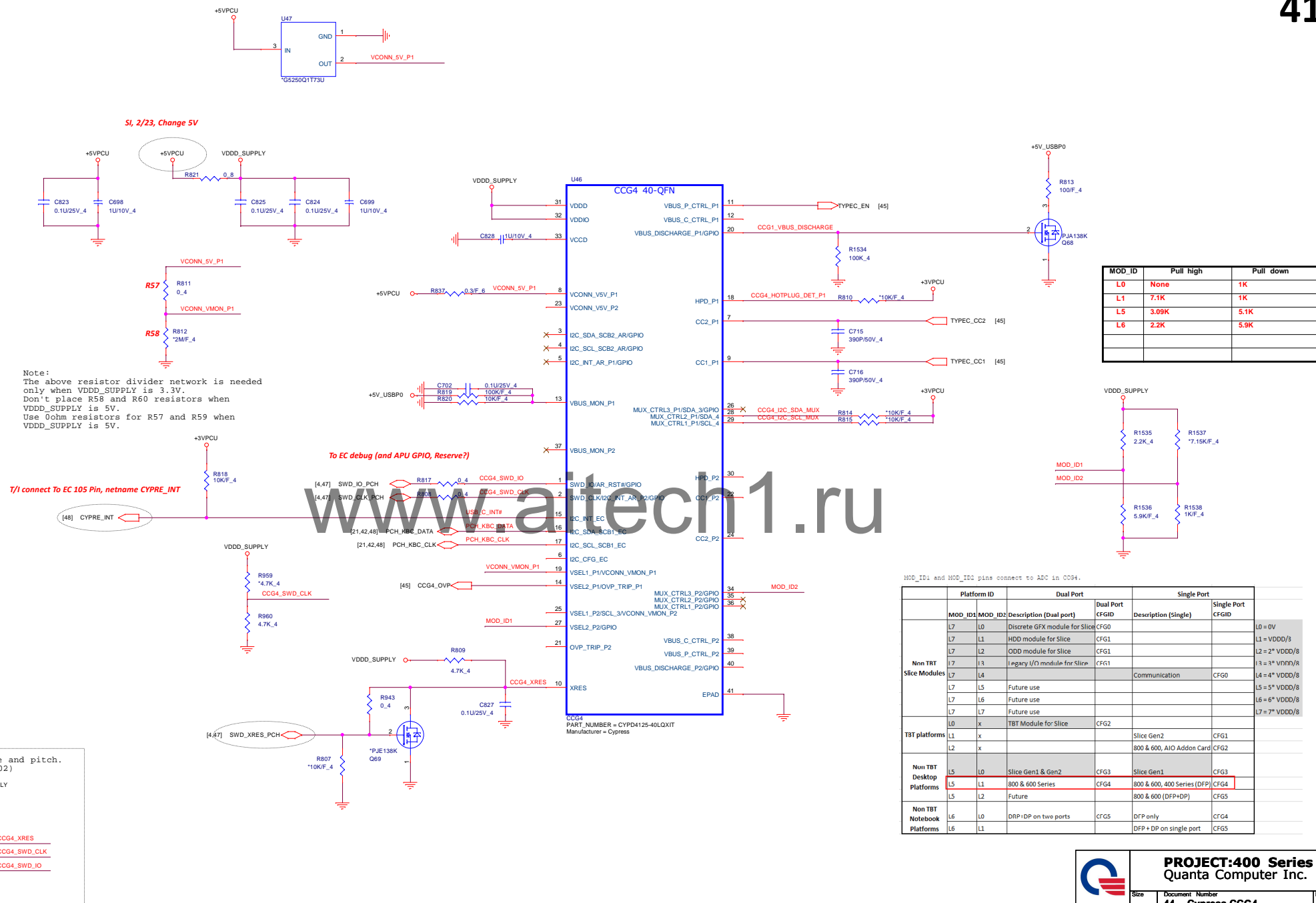
12S RESET MODE INSTAL FOR DB0		
INSTAL	R10702 R10704 R10701 U9068	R1070 R? R?
UNINSTAL	R? Q7080	R? Q7081

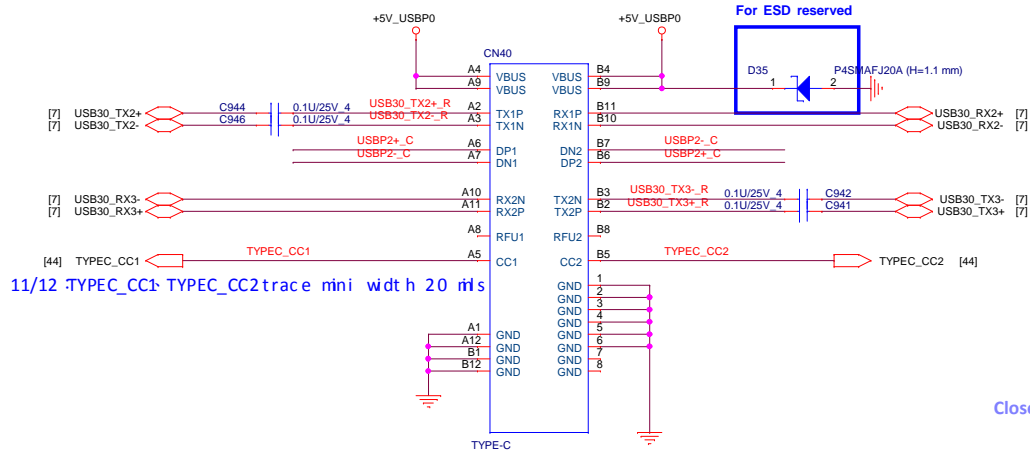
[2,3,4,5,7,8,9,10,16,17,18,19,20,24,26,27,29,30,31,33,34,36,38,39,42,43,46,47,48,50,52,57,59,60,64,67] +3V
[8,27,29,30,40,42,43,55,59,64,67] +5V
[9,51,52,53,59,63,64,67] +3V_ALW



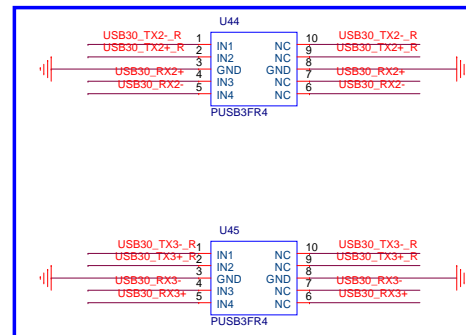
SATA-HDD



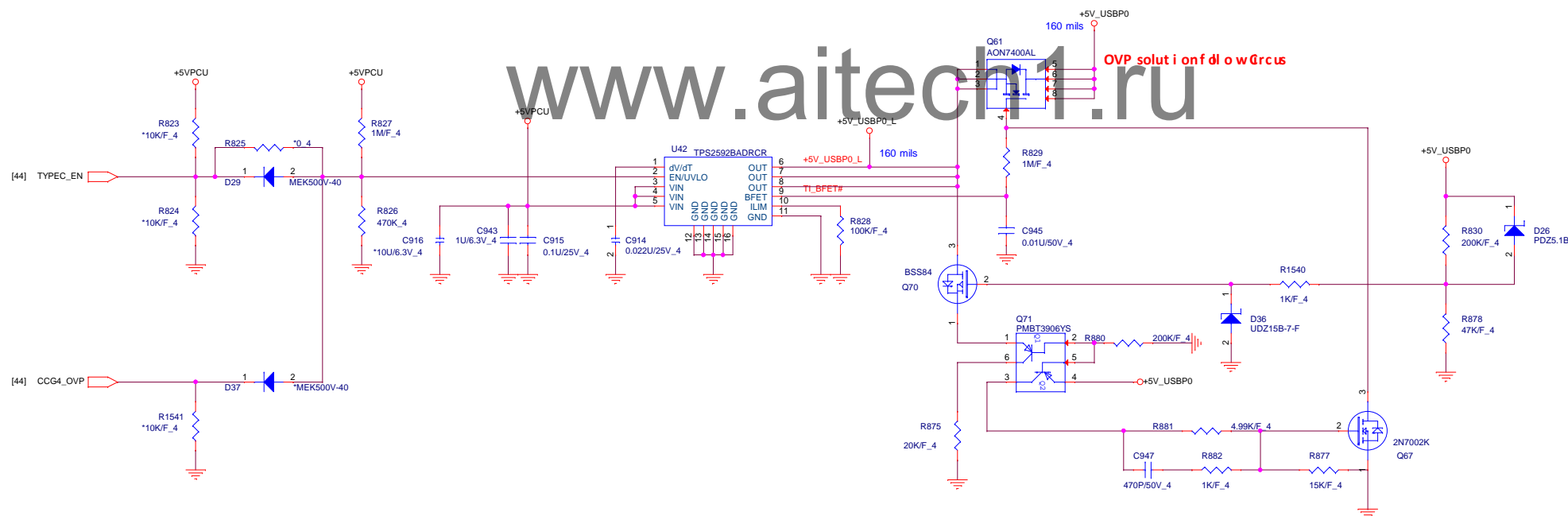
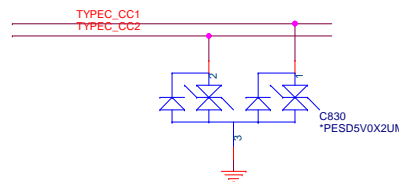
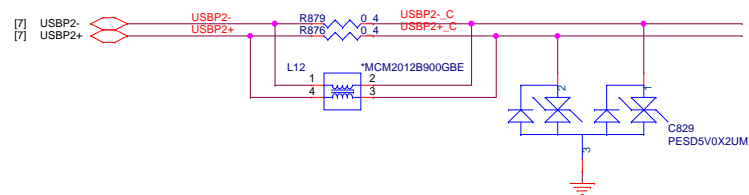
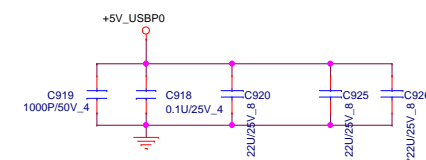


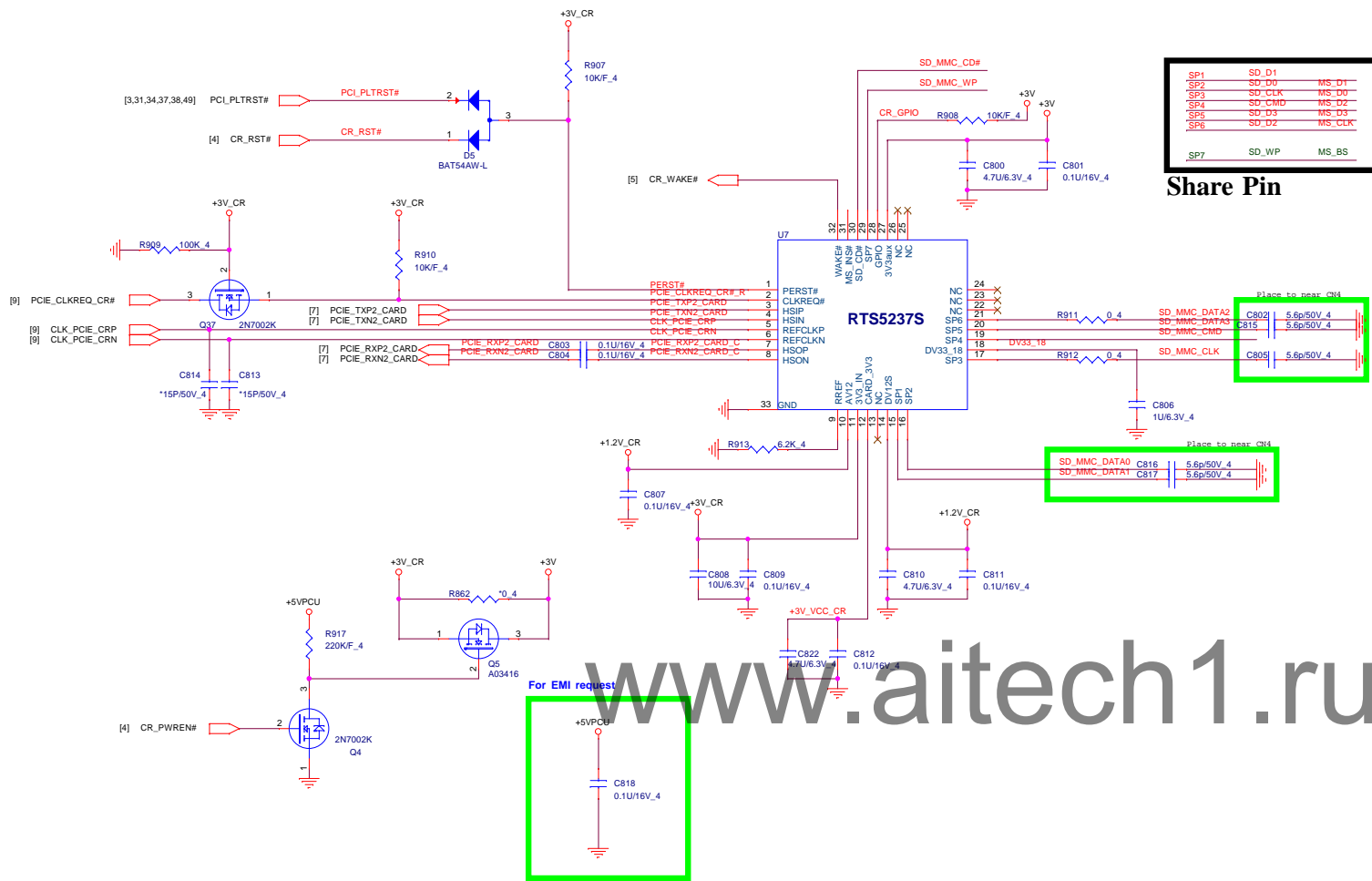


Reserve ESD chip



Close CN40



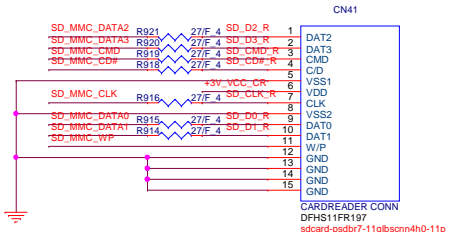


SP1	SD_D1	MS_D1
SP2	SD_D0	MS_D0
SP3	SD_CLK	MS_D0
SP4	SD_CMD	MS_D2
SP5	SD_D3	MS_D3
SP6	SD_D2	MS_CLK
SP7	SD_WP	MS_BS

Share Pin

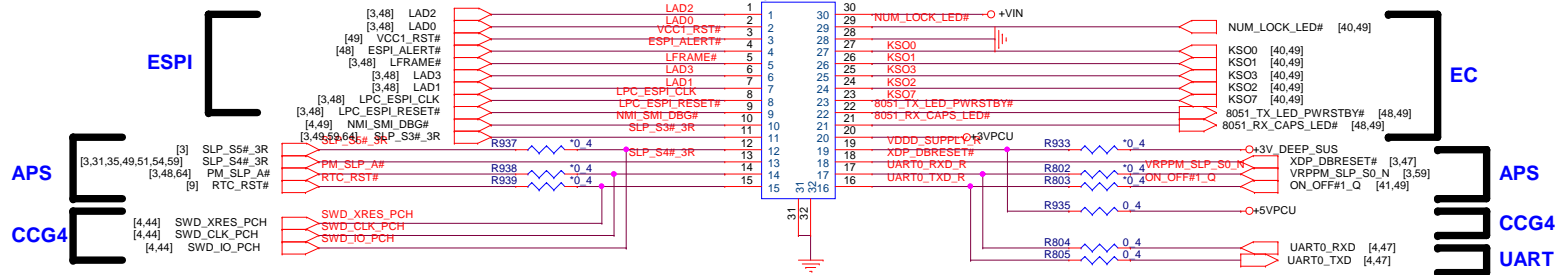
Place to near CH4

Place to near CH4

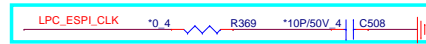


ESPI+EC+APS debug conn on MB

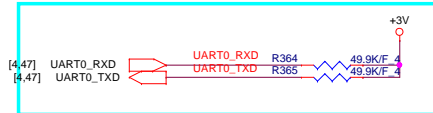
debug_CONN_30P
CN14



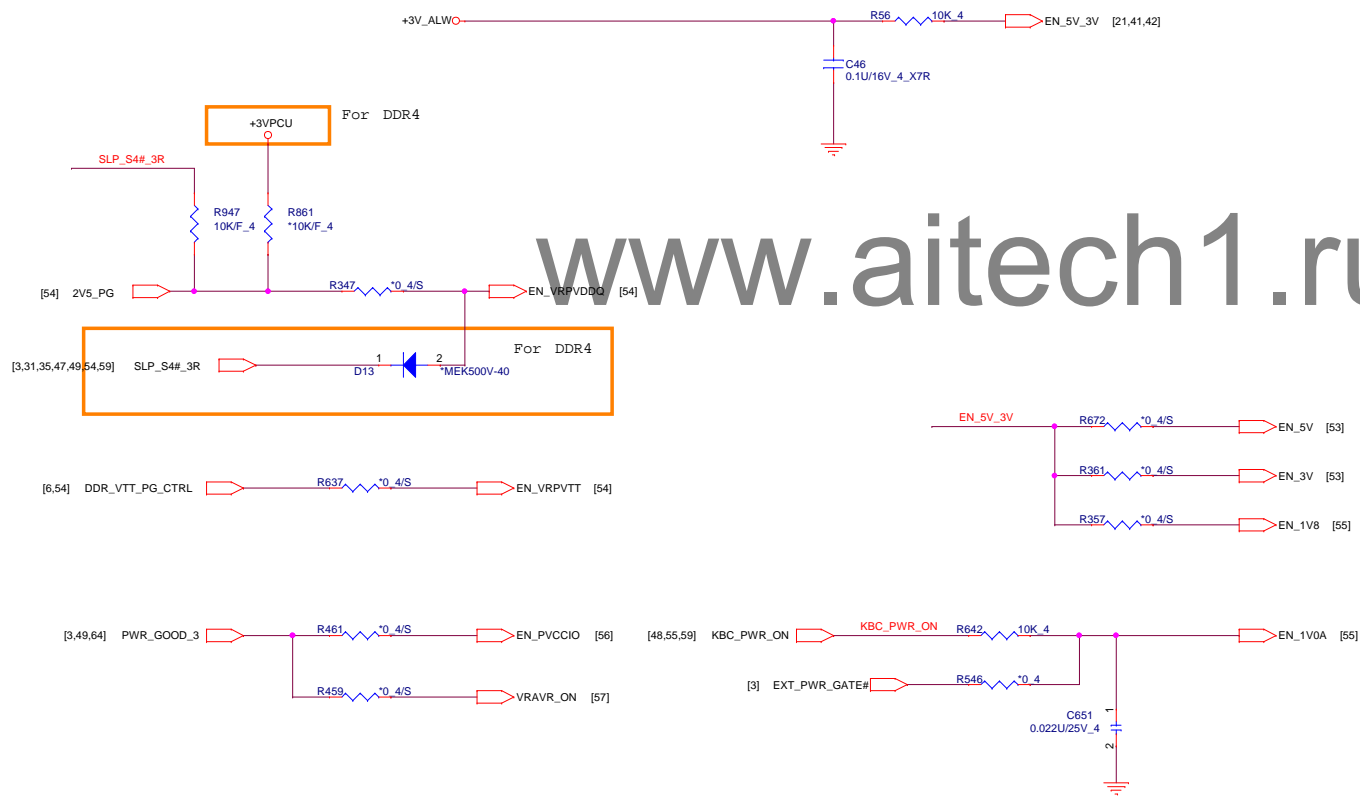
For EMI reserved



For check list

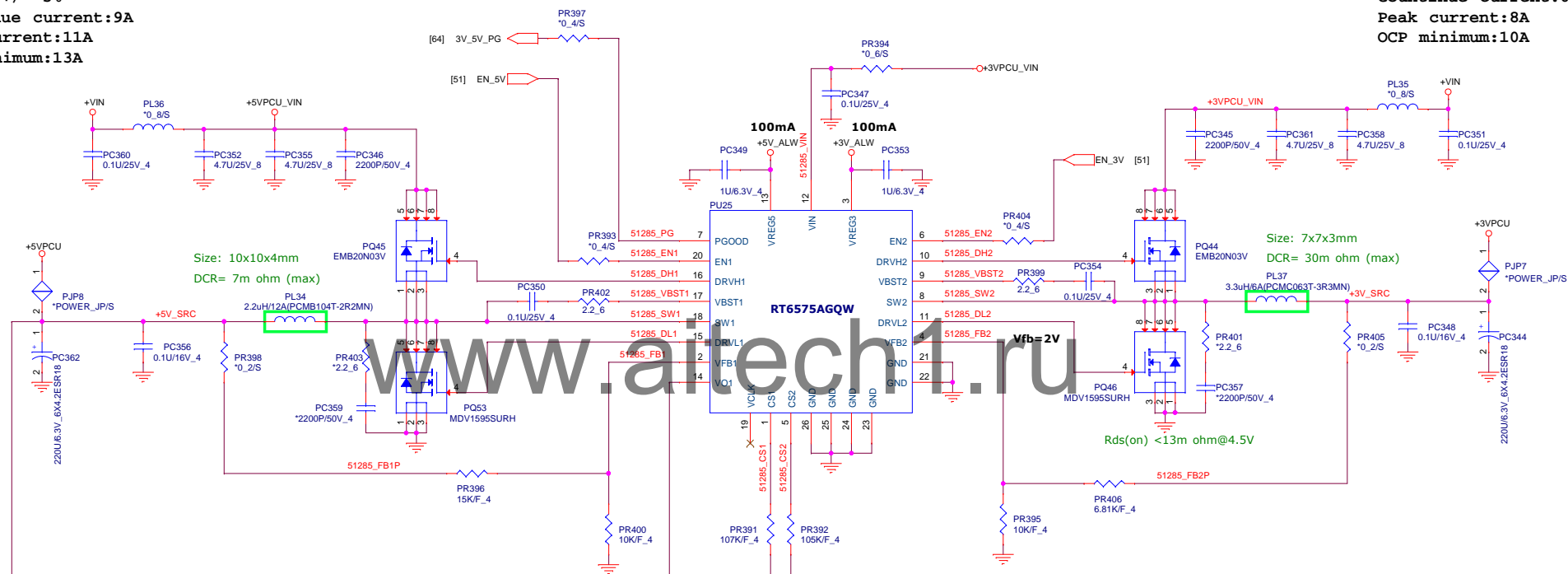


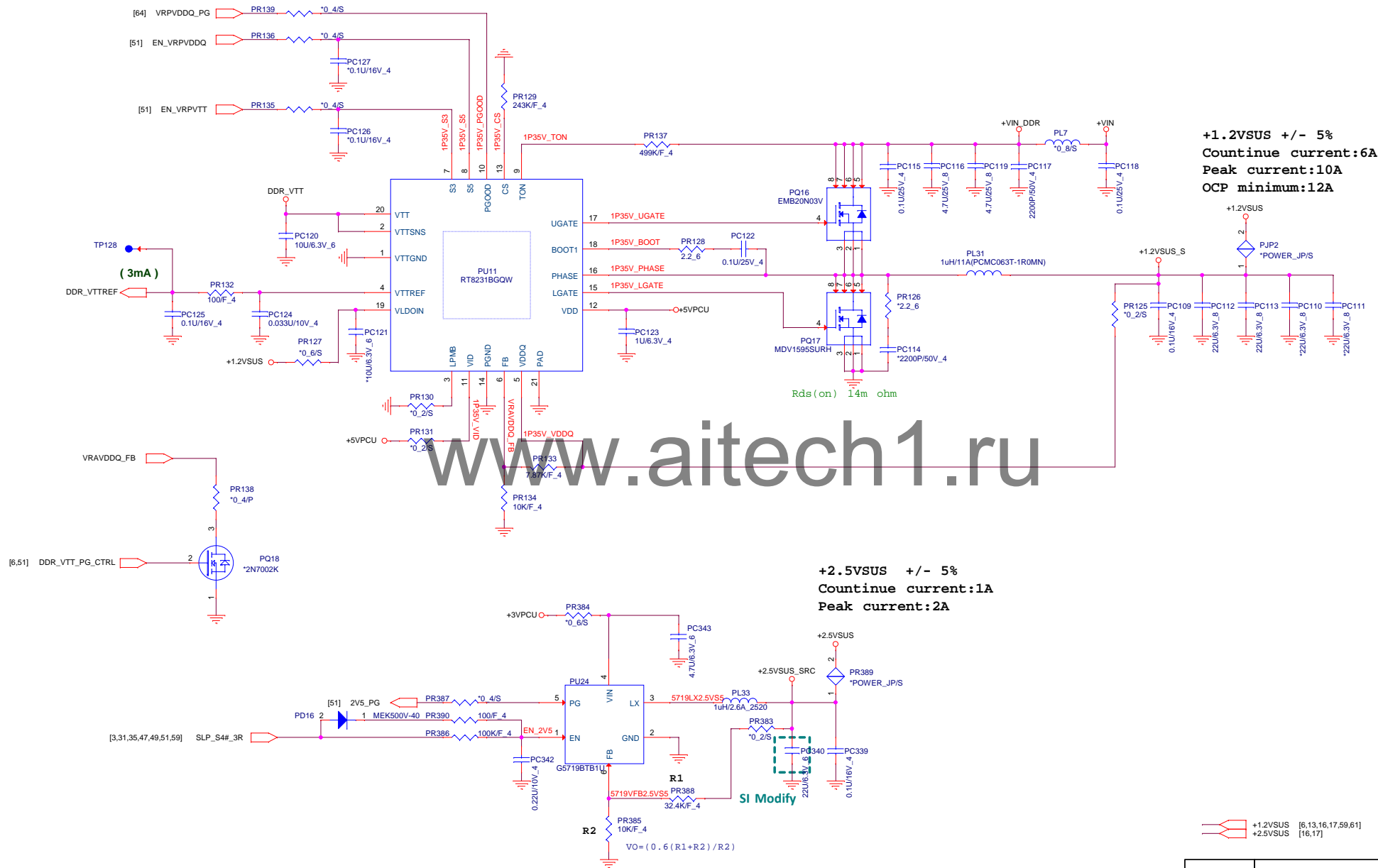
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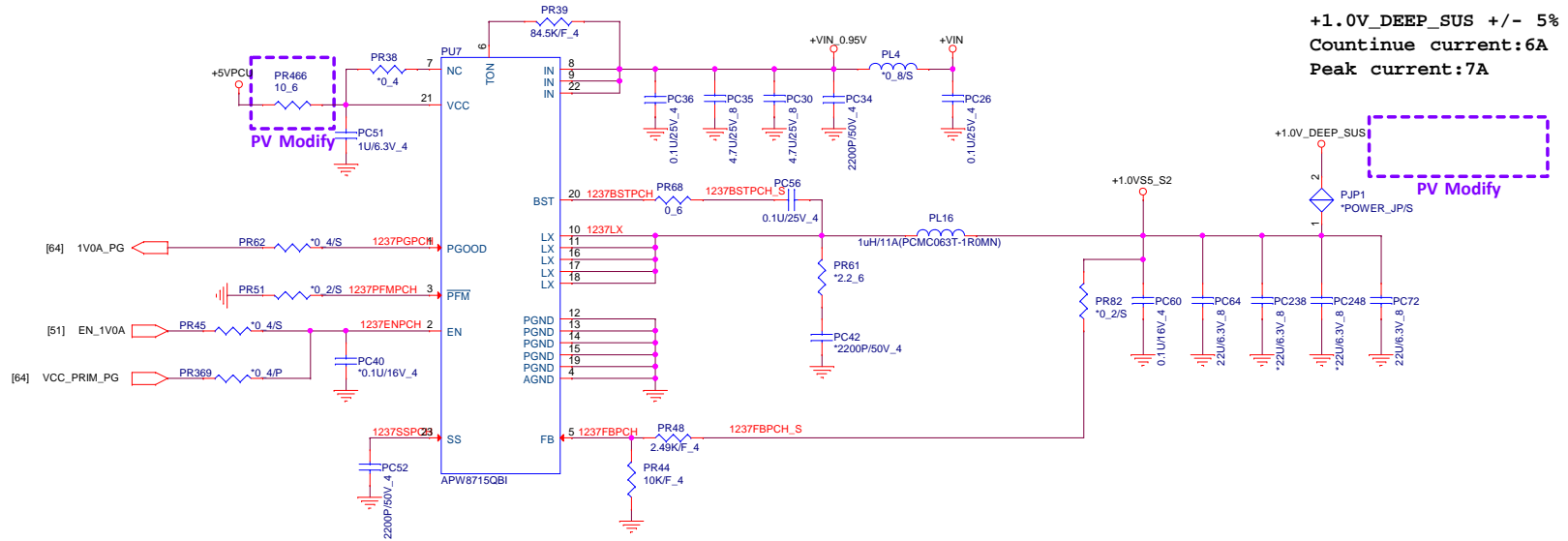




+3VPCU +/- 5%
Continue current:6A
Peak current:8A
OCP minimum:10A

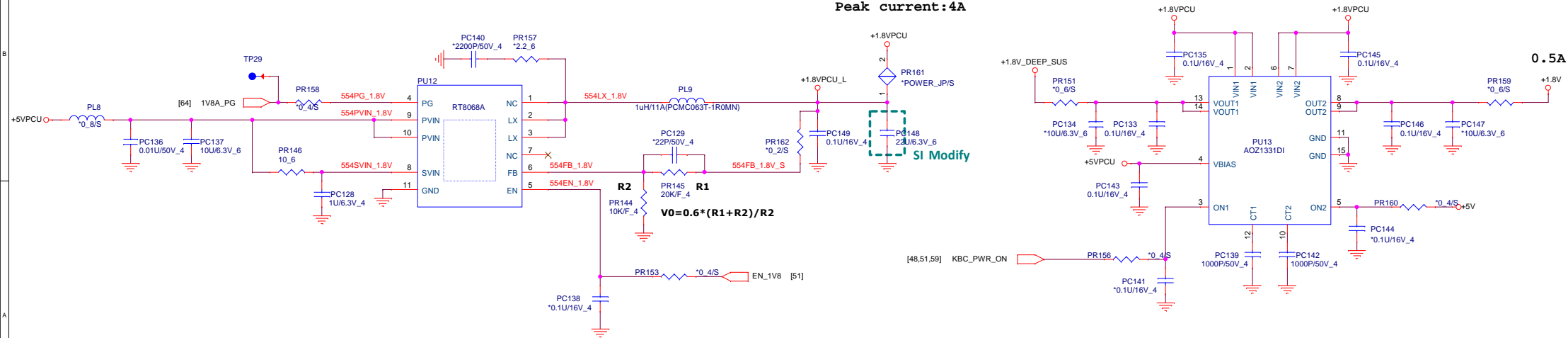






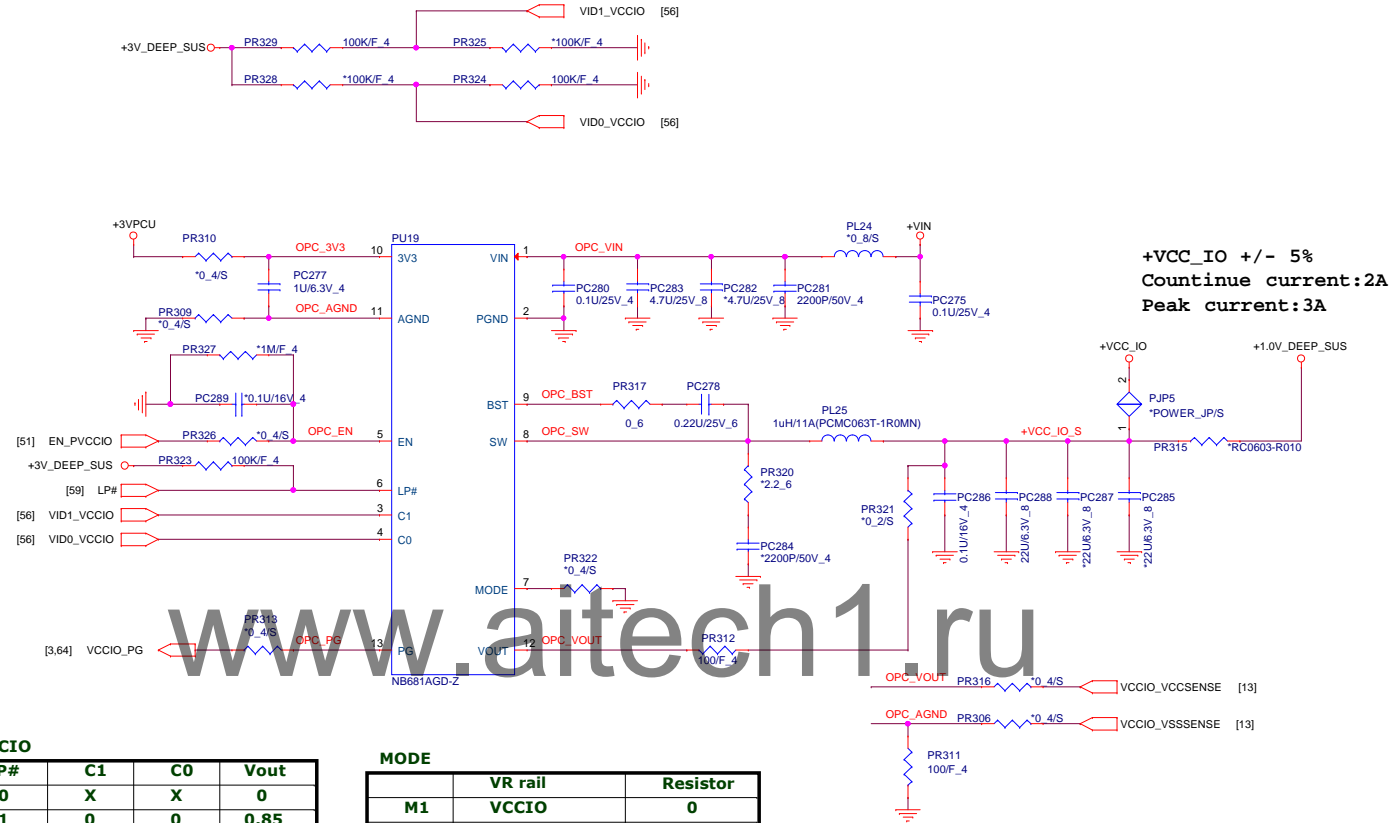
www.aitech1.ru

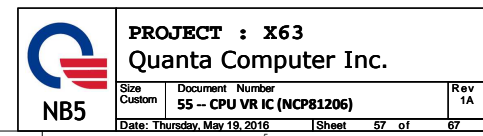
+1.8VPCU +/- 5%
Countinue current:2A
Peak current:4A

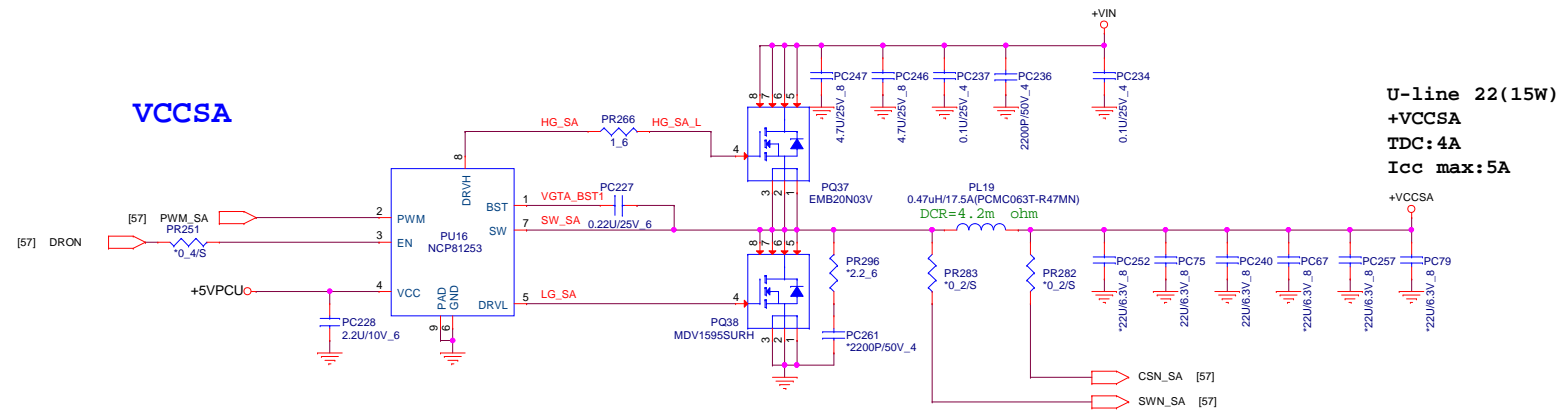


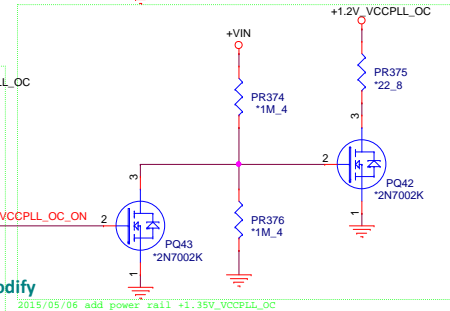
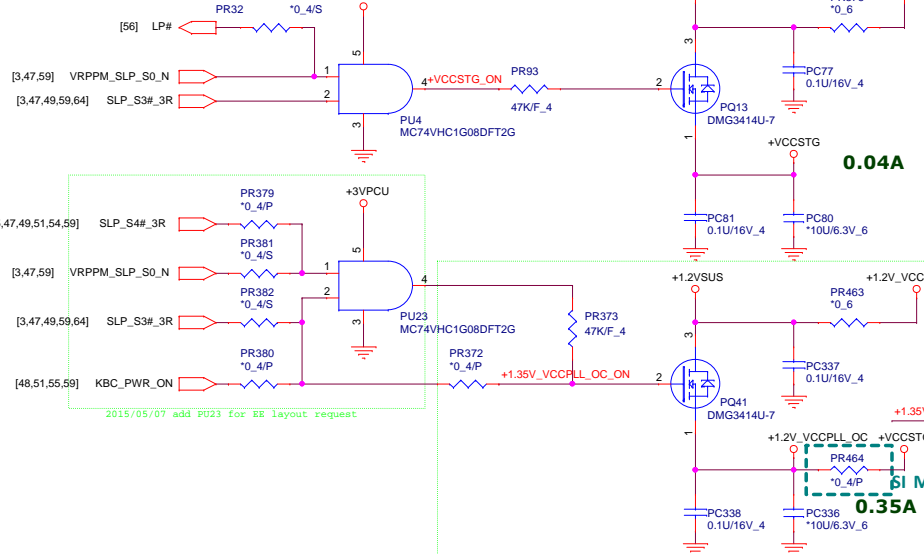
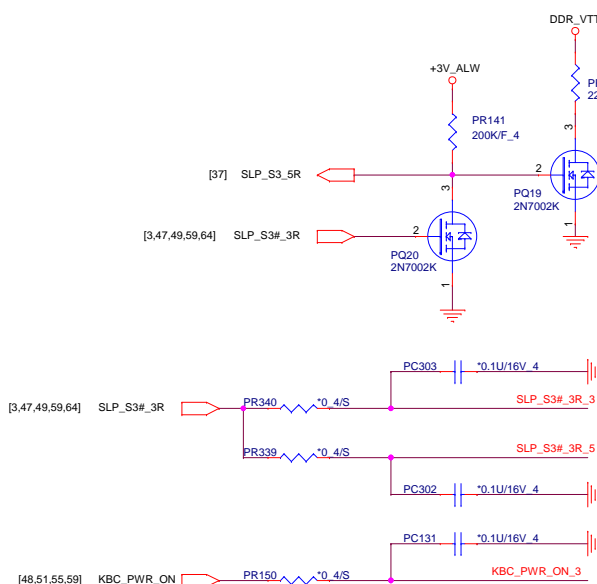
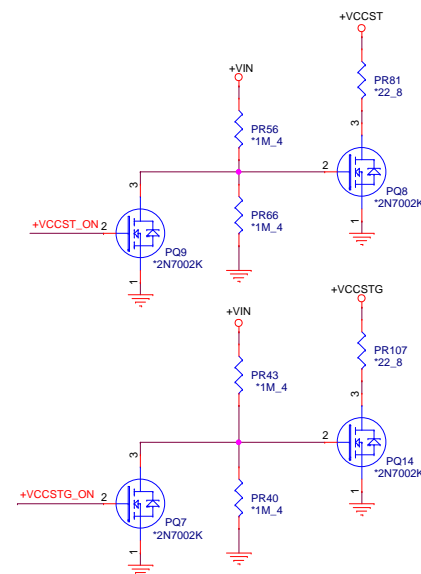
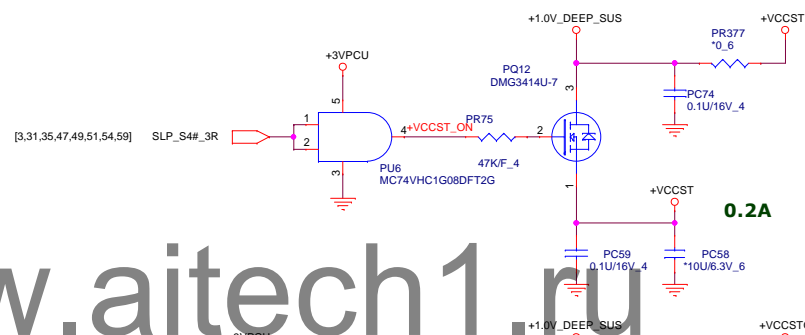
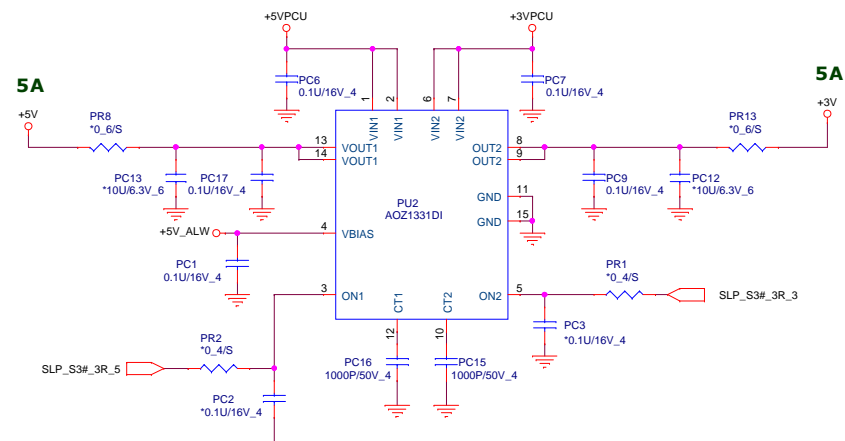
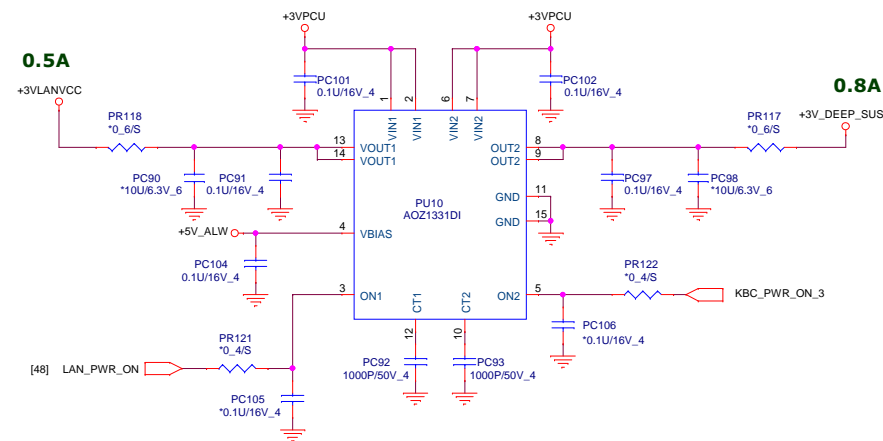
+VIN [26,43,47,52,53,54,56,57,58,59,60,62,67]
+3VPCU [3,10,33,37,38,40,41,42,44,47,48,49,51,52,53,54,56,59,61,63,64,67]
+5VPCU [31,35,44,45,46,47,52,53,54,57,58,59,60,61,62,64,67]

[26,43,47,52,53,54,55,57,58,59,60,62,67] +VIN
[9,41,51,52,53,59,63,64,67] +3V_ALW
[5,13] +VCC_IO





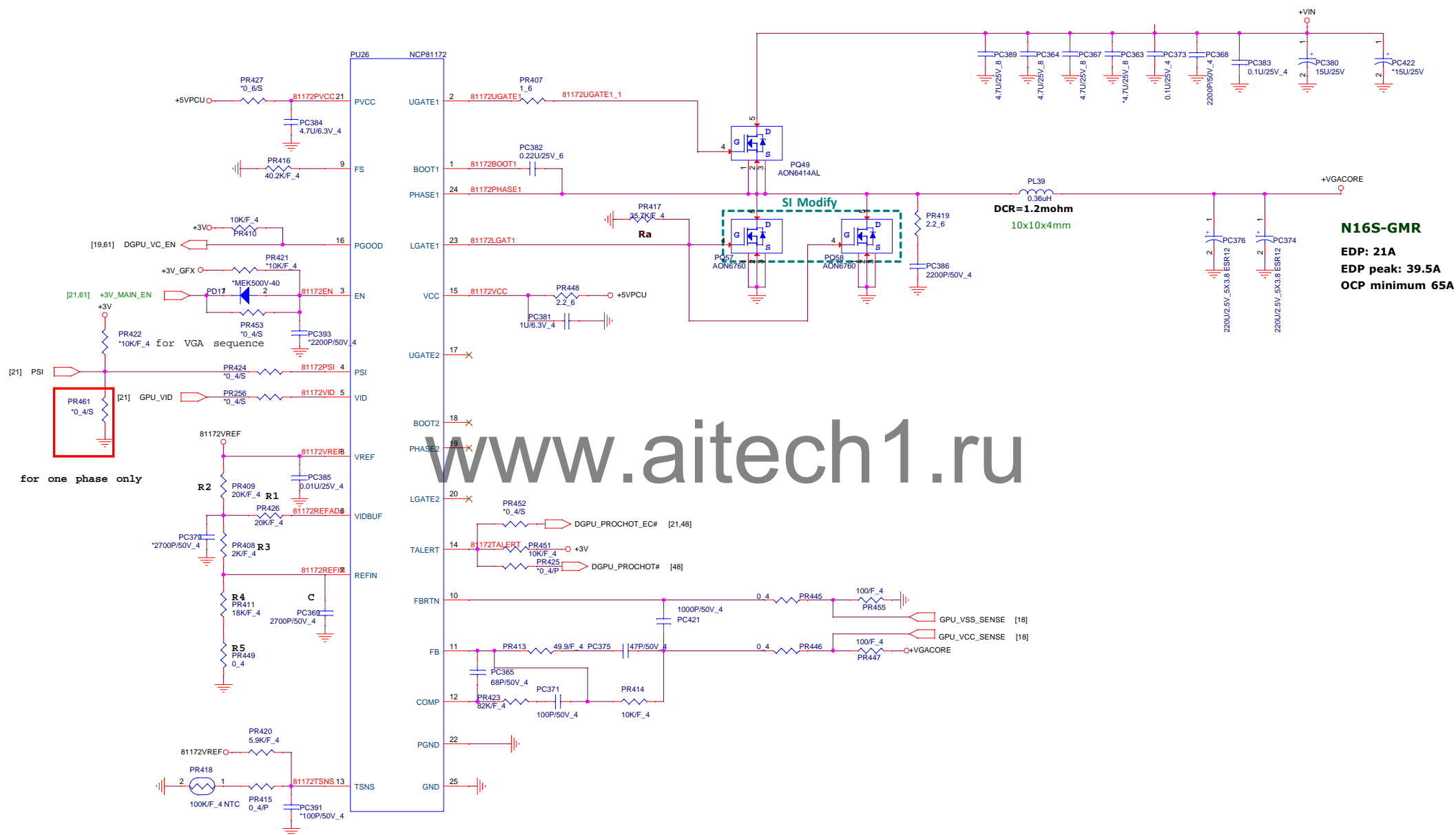


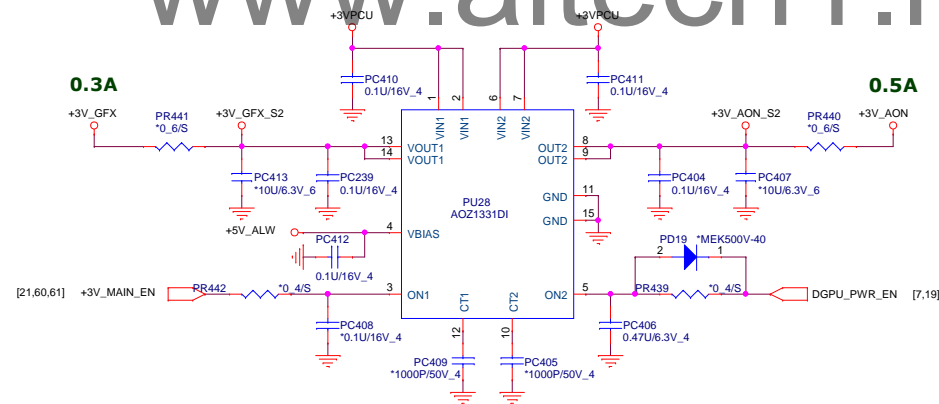
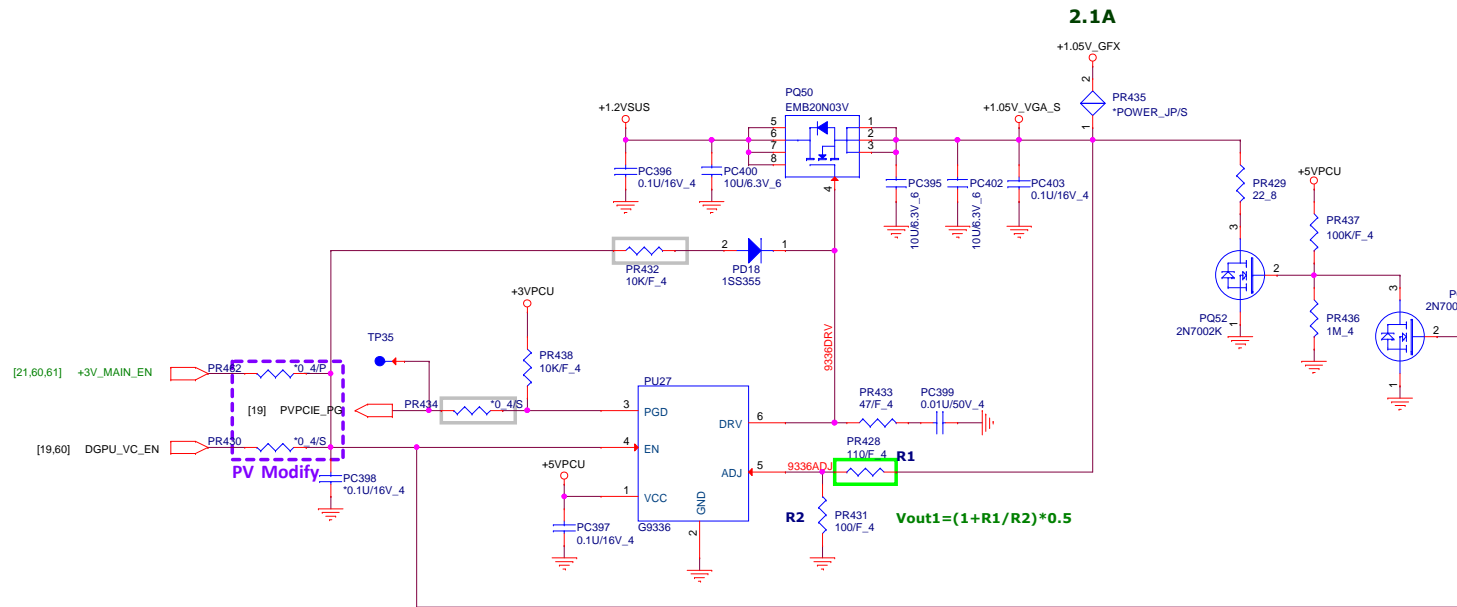


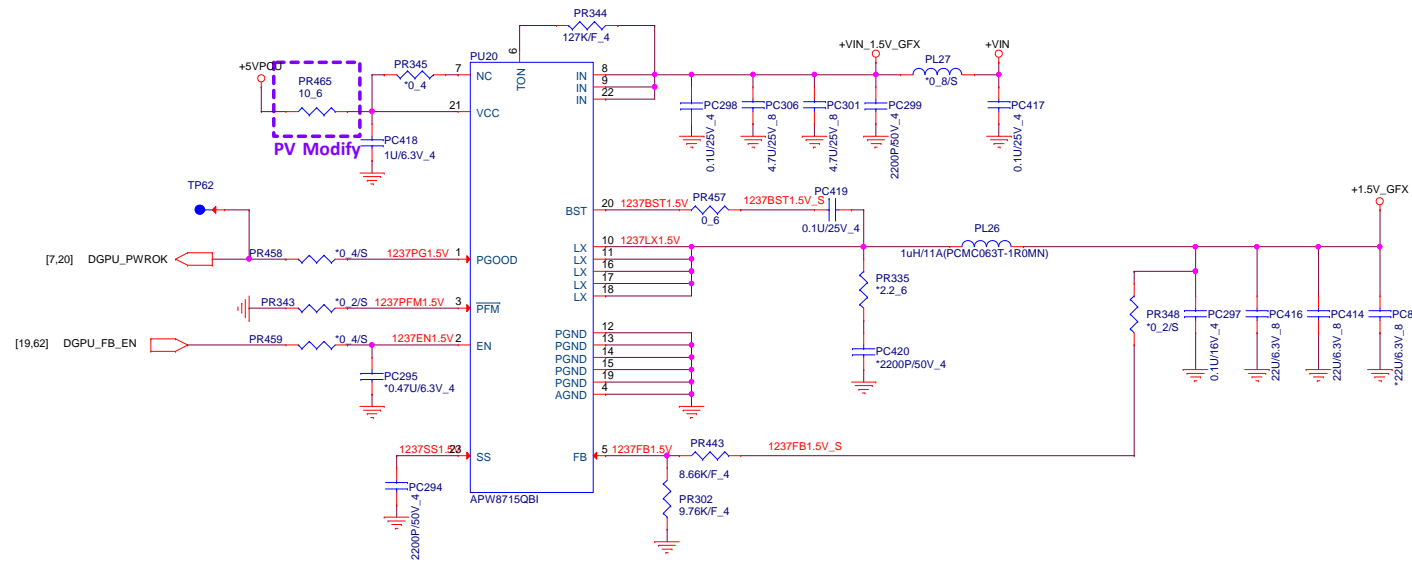
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 [31,35,44,45,46,47,52,53,54,55,57,58,60,61,62,64,67]
 [31]

PROJECT : X63		Quanta Computer Inc.	
Size	Document	Number	Rev
Custom	57	Load switch IC (APL3523A)	1A
Date: Thursday, May 19, 2016	Sheet	59 of	67

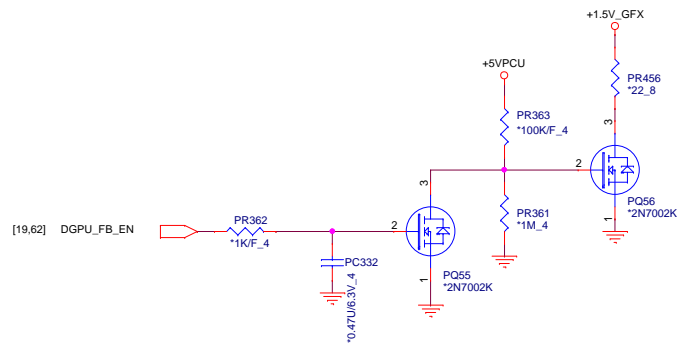




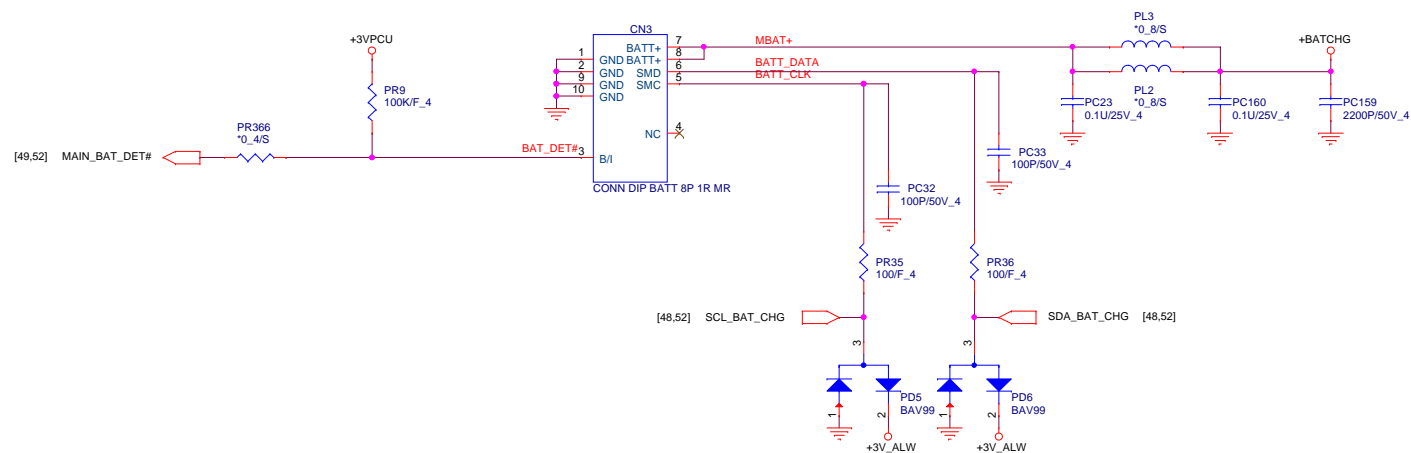
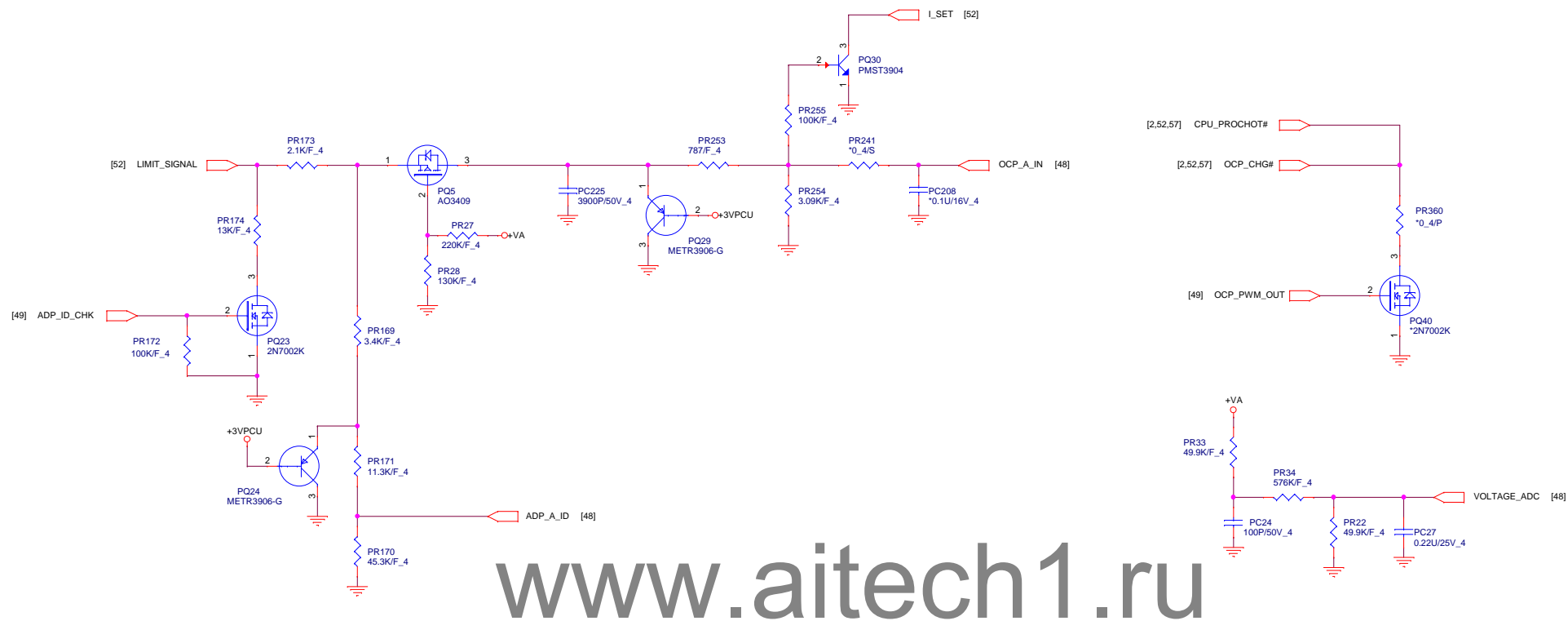




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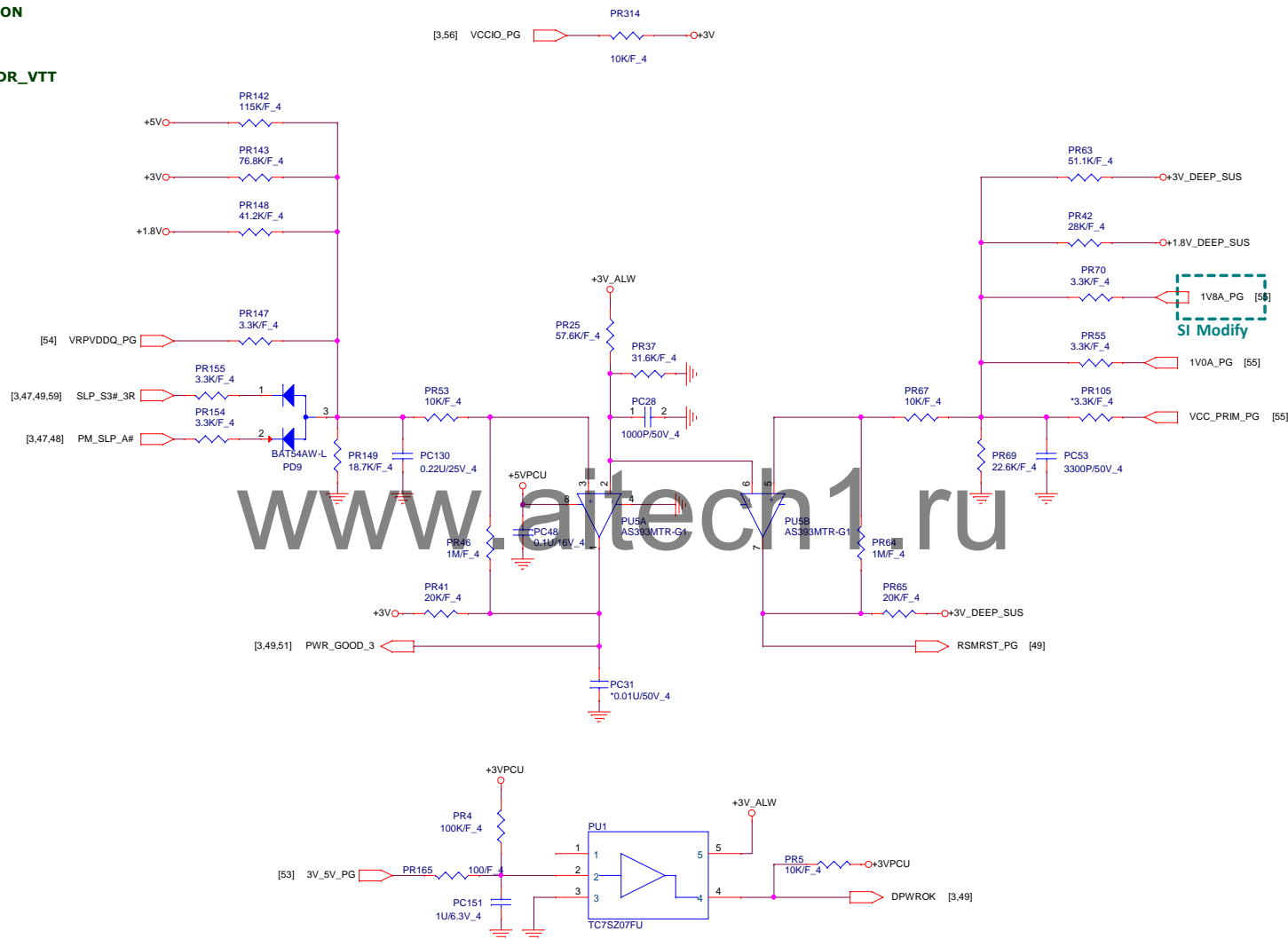


Adapter OCP

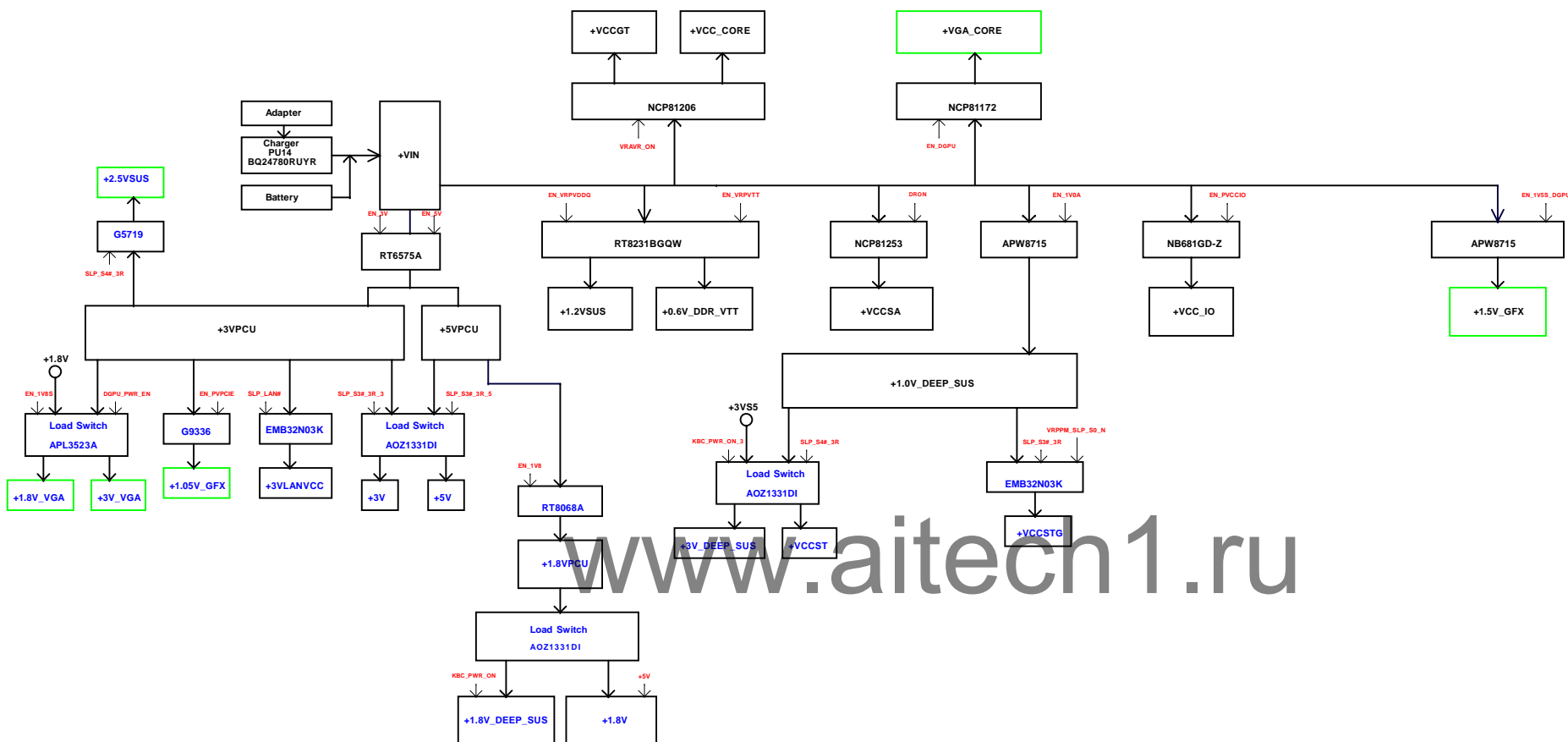


POK CKT

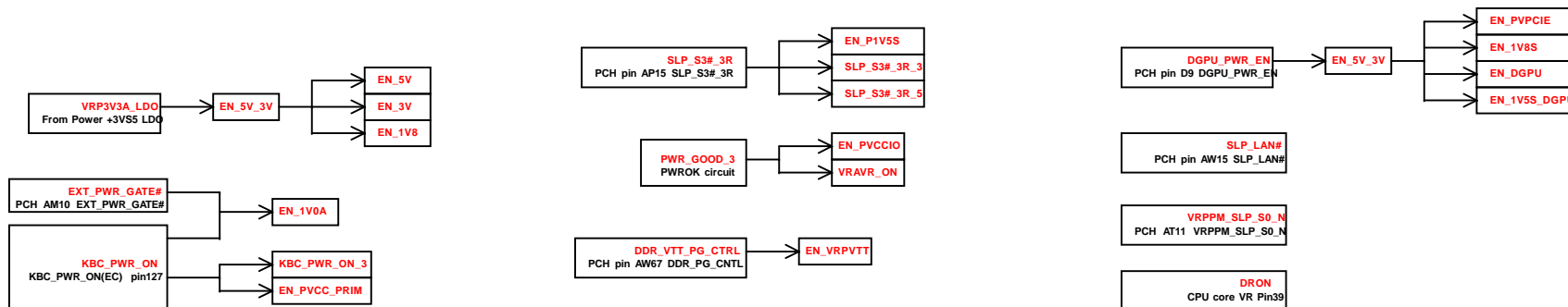
```
PM_SLP_S4# = SUSON
PM_SLP_S3# = MAINON
+V5S = +5V
+V3S = +3V
+V0.75S = +0.75V_DDR_VTT
```



POWER BLOCK DIAGRAM

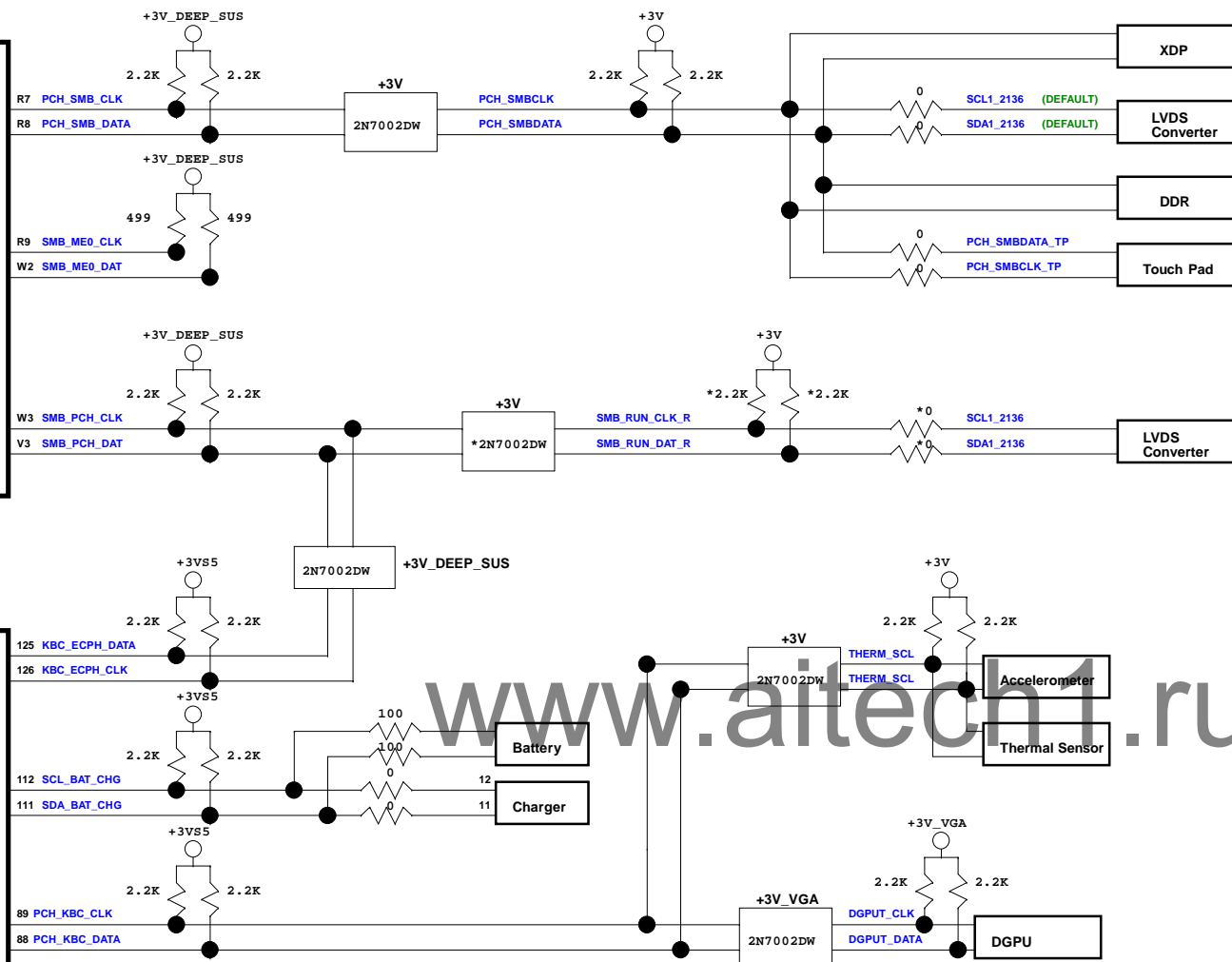


POWER ENABLE PIN



SKYLAKE U

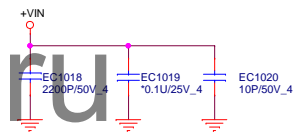
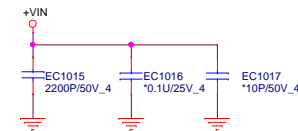
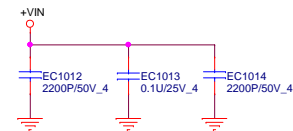
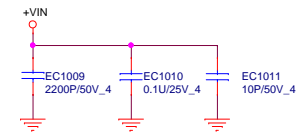
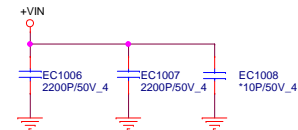
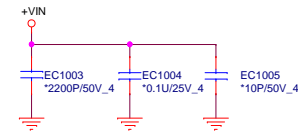
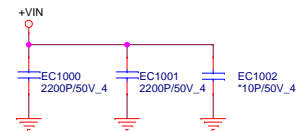
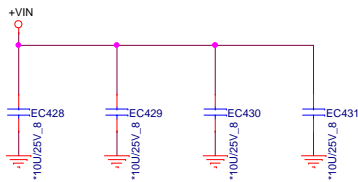
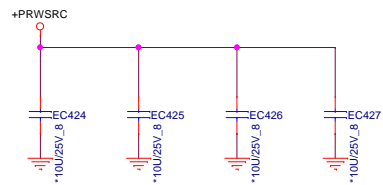
EC
NPCE586H



Example: *499/F_4 and *0_6/S
 * means none-installed
 499 means value
 F means 1%
 _4 means 0402 size
 /S means short pad

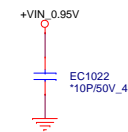
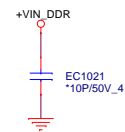
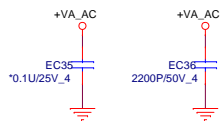
Mult i plexed HSIO Lane	Port Assignment
USB3 #1	USB2.0/USB3.0 Combo Jack(Lef t s i de do wn)
USB3 #2 / SSIC #1	USB2.0/USB3.0 Combo Jack(Lef t s i de up)
USB3 #3 / SSIC #2	NC
USB3 #4	NC
PCIE1 / USB3 #5	dGPU
PCIE2 / USB3 #6	dGPU
PCIE3	dGPU
PCIE4	dGPU
PCIE5	LAN
PCIE6	WLAN
PCIE7 / SATA #0	HDD (SATA)
PCIE8 / SATA #1	ODD (SATA)
PCIE9	Cardreader (PCIE)
PCIE10	NC
PCIE11 / SATA #1*	NC
PCIE12 / SATA #2	SSD (SATA)

USB2.0	Port Assignment
USB2 #1	USB2.0/USB3.0 Combo Jack(Lef t s i de do wn)
USB2 #2	USB2.0/USB3.0 Combo Jack(Lef t s i de up)
USB2 #3	WWAN
USB2 #4	USB2.0(Right side on USB Board)
USB2 #5	USB2.0(Right side on USB Board)
USB2 #6	Touch Screen
USB2 #7	Bluetooth
USB2 #8	Finger Print
USB2 #9	Camera
USB2 #10	NC

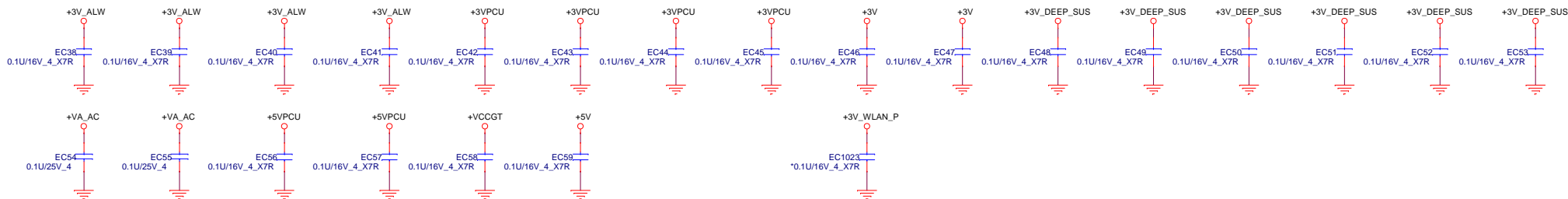


EMI cap

RF cap



EMI cap



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